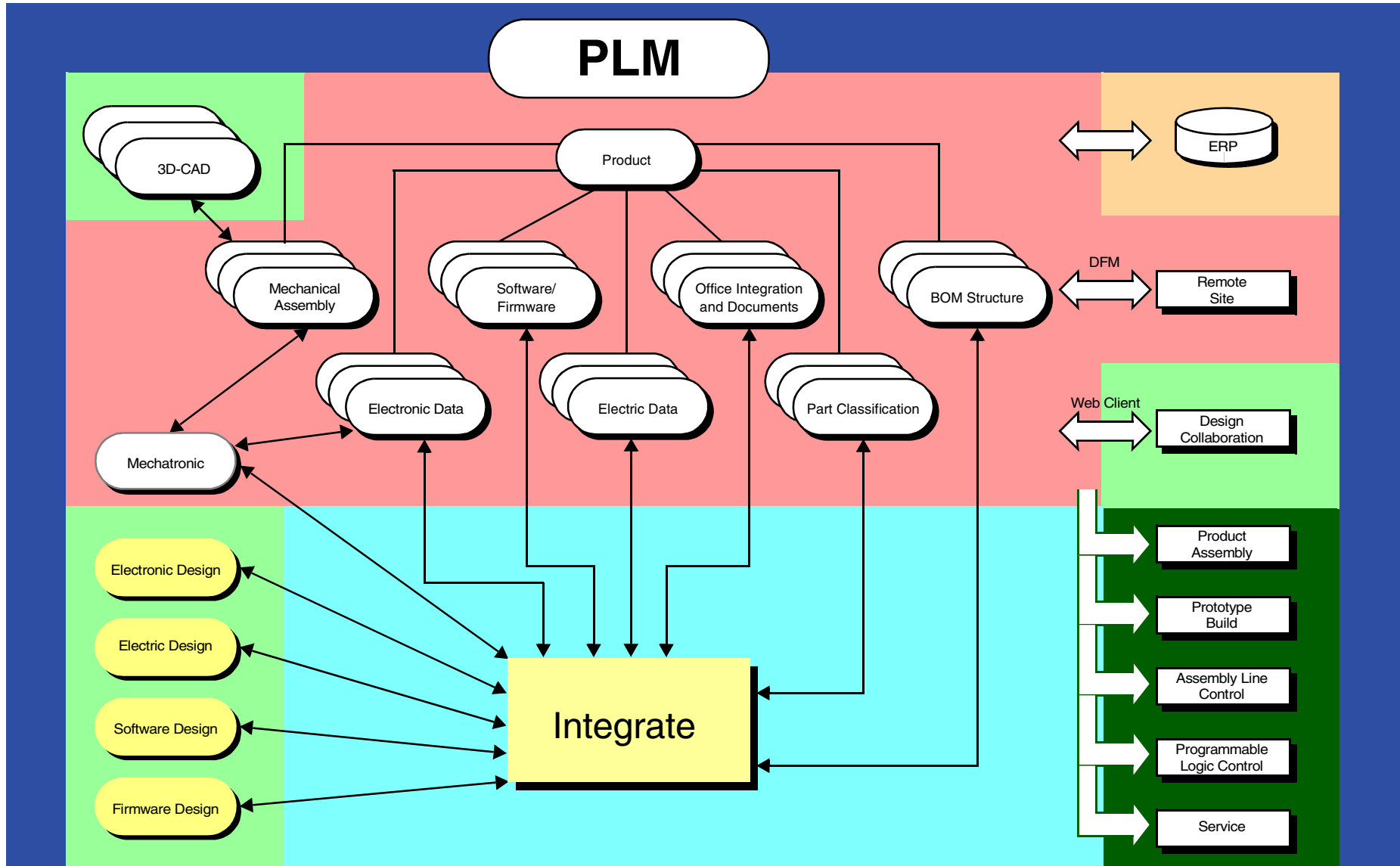


Data Processing and Distribution



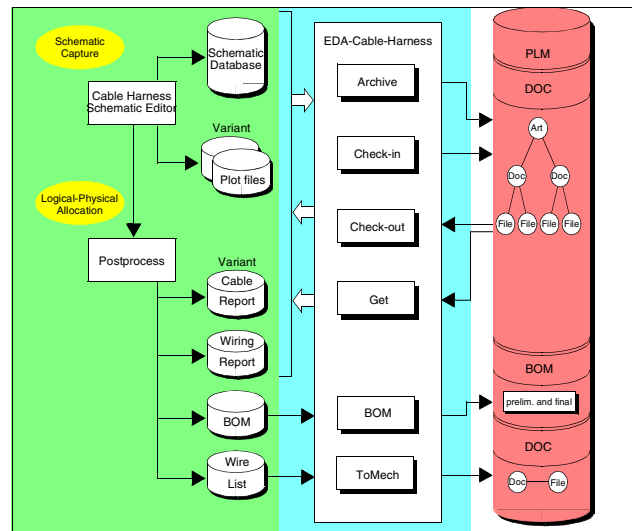
PLM with Electric Design

EDA-Cable-Harness integrates the leading electric and harness capture tools with the PLM systems. PLM provides the backbone of data configuration, project and workflow management services essential to the successful automation and control of the electrical system data and processes.

The **EDA-Cable-Harness** module supports the electric and harness design processes with variants, report files and the integration with the mechanical interface. Management of workgroup, enterprise and external communications are enhanced through the inherently distributed architecture of the PLM system. Features include the automatic extraction of BOM's, of reports, plot files, and the support of design derivatives.

The **EDA-Cable-Harness** interface is based on the JAVA® IUI and works across many platforms. It is integrated with other PLM modules such as the PLM

BOM module, Project Management [or PPM], and Product Collaboration.



Functionality

- ✓ **Synchronize Parts** Optionally bidirectional synchronisation of component data with PLM. This includes release control, component grading, and part usage cross references.
- ✓ **Check-in** Check-in of design data and reports with user defined file level resolution, along with the check and creation of metadata. Data, library and post-processing files are linked to a versioned document in the PLM system and configured together with mechanical and product documentation for a complete, versioned representation of product data.
- ✓ **Check-out** Search and retrieval of design data, with all dependencies, directly from the PLM system into the EDA working environment. Any of the PLM system attributes can be used to search for the desired design, and with appropriate permissions any version of the design can be retrieved to perform an engineering change.
- ✓ **BOM** The product BOM is automatically extracted and managed in the PLM system for later transfer to MRP/ERP systems. The variant PLM BOM contains Designator and Location data from the harness design system and, optionally, wire and component attributes.
- ✓ **Process** **EDA-Cable-Harness** uses the PLM release procedures and workflows to manage the state of logic design data. Engineering Change Request workflows and communications with vendors and manufacturing are easily implemented.
- ✓ **Variant** Includes support of design derivatives from a common pool to allow efficient design and manufacturing of families of products.
- ✓ **Tailorable** The data model, process flows, and release procedure steps can be configured on-site to match company specific business practices.

Integrate

Benefits

- * Cross-team design coordination. Concurrent engineering can span workgroups and continents!
- * Design release process control. Manufacturing and Vendors receive the right data... the first time!
- * Simplifies compliance with ISO9001, ISO10007, QSA9000, FDA and GMP guidelines!
- * Bill-of-Materials extraction includes the automatic generation of hierarchical manufacturing BOMs.
- * Automatic extraction and check-in of schematics, cable lists, connector lists and other reports and plot files configurable for your companies' needs.
- * Check-in of design derivatives based on a sum design supported with association of specific product ids in PLM.
- * Works unobtrusively within the familiar electric tool user interface, so engineers can concentrate on their design activities.
- * Significant benefits in data security, handling of mass data, and speed up of the design process.

Supported Systems

Cable Harness logic design systems like Logic Cable® of Mentor Graphics, ELCAD®, Eplan®, Ruplan®, Promis, ecscad®, ProPlan®, e³series®, and many others. **EDA-Cable-Harness** is available with the operating systems Windows NT 4.0, 2000+, and XP.

Options

- **EDA-Librarian** for electric library management including control of component part numbers and attributes, wire part numbers and attributes, part status, and library release processes.
- System design process and data flow automation such as: back-annotation of PLM system BOM changes based on Part Number or property changes into the design data, and automatic maintenance of component attribute files.
- Inspect the “intelligent” viewer and analysis tool of schematic and layout data. Empower the shop floor and the laboratory with cross probing, lookup of component parameters, connector , and net tracing, etc., from a platform independent JAVA window without the expense of an EDA application license.

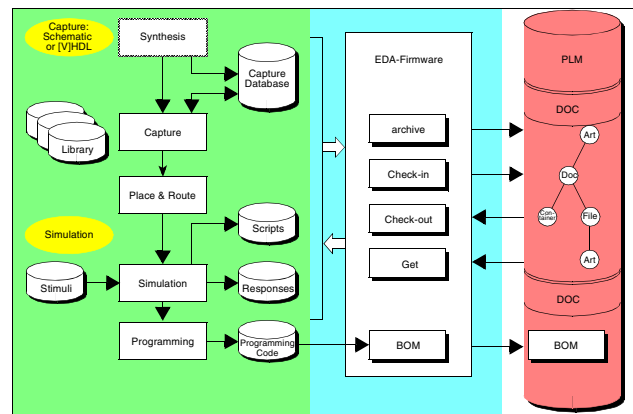
Integrate®

PLM with Programmable Logic Systems

EDA-Firmware integrates the leading Programmable Logic Design tools for processor code design, PLD design, and FPGA design with the PLM systems. PLM provides the backbone of data, configuration, project and workflow management services essential to the successful association and control of the firmware design data and processes.

The **EDA-Firmware** module supports integration of Programmable Logic design environments with the design's process flow. Association of programming code to electronic items is performed in PLM. Engineering changes and variants caused by firmware revisions are supported. Workgroup, enterprise and external communications are enhanced through the inherently distributed architecture of the PLM system. Features include the automatic extraction and download of programming code files and the implementation of printed circuit board variants based on firmware versions.

The **EDA-Firmware** interface is based on the JAVA® IUI and works across many platforms. It is integrated with other PLM modules such as the PLM BOM module, Project Management [or PPM], and Product Collaboration.



Functionality

- ✓ **Check-in** Check-in of design environment with user defined file level resolution, along with the check and creation of metadata. Data and programming code files are linked to a versioned Document in the PLM system and configured together with hardware design data for a complete, versioned representation of product data.
- ✓ **Check-out** Search and retrieval of the design environment, with all dependencies, directly from the PLM system into the firmware design environment. PLM system attributes can be used to search for the desired design, and with appropriate permissions, any version of the design can be retrieved to perform an engineering change.
- ✓ **Process** **EDA-Firmware** uses the PLM release procedures and workflows to manage the state of design data. Engineering Change Request workflows and product state reports support time-to-market decisions.
- ✓ **Variants** Support of firmware-based variants of the electronic assembly to allow efficient design and manufacturing of families of products.
- ✓ **Tailorable** The data model, process flows, and release procedure steps can be tailored on-site to match company specific business practices.

Integrate

Benefits

- * Cross-team design coordination. Concurrent engineering can span workgroups and continents!
- * Design release process control. Manufacturing and Vendors receive the right data... the first time!
- * Simplifies compliance with ISO9001, ISO10007, QSA9000, FDA and GMP guidelines!
- * Integration of all sorts of programmable logic design environments like In-system programming, FPGA, and PLD design.
- * Automatic extraction and check-in of the design data for engineering changes and revision spins.
- * Check-in of programming code files and association with specific components in electronic designs and products.
- * Version and variant control linked to data from the electronic design system at any time.
- * Significant gains in data security through revision association of programming code and electronic hardware.
- * Works unobtrusively within the familiar design user interface, so engineers can concentrate on their design activities.

Supported Systems

Firmware design systems of Altera®, Actel®, Intel®, Xilinx®, LatticeLogic®, Motorola®, Texas Instruments®, Renoir® of Mentor Graphics®, and many others. Integrate-Firmware is available with the operating systems Solaris 2.5.1,-2.8, HP-UX 10.20, HP-UX 11, Windows NT 4.0, Windows 2000+, and XP.

Options

- **EDA-Logic** and **EDA-Layout** to automate the electronic design and design process and to build consistent, accurate product configurations within the PLM system.
- Inspect the “intelligent” viewer and analysis tool of electronics data. Empower the firmware designer, shop floor, and the laboratory with cross probing, lookup of components and component parameters, net tracking, etc., from a platform independent window without the expense of an EDA application license.

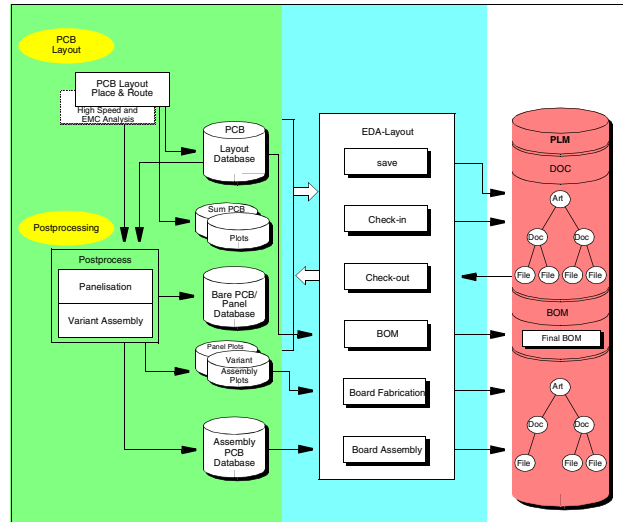
Integrate®

PLM with Printed Board Layout

EDA-Layout integrates the leading EDA-PCB-Layout tools with the PLM system. PLM provides the backbone of data, configuration, project and workflow management services essential to the successful automation and control of the EDA-PCB-Layout data and processes.

The **EDA-Layout** modules automate the task of module based PCB design and data management. Workgroup, enterprise, and external communications are supported through the inherently distributed architecture of the PLM system. Features include the automatic extraction of manufacturing data BOM's and attributes and the full support of assembly and programming variants.

The **EDA-Layout** interface is based on the JAVA® UI and works across many platforms. It is integrated with other PLM modules such as the PLM BOM module, Project Management [or PPM], and Product Collaboration.



Functionality

- ✓ **Check-in** Check-in of design data with user defined file level resolution, along with the check and creation of metadata. Data, library and post-processing files are linked to a versioned Document in the PLM system and configured together with mechanical and product documentation for a complete, versioned representation of product data.
- ✓ **Check-out/Get** Search and retrieval of design data, with all dependencies, directly from the PLM system into the EDA working environment. Any of the PLM system attributes can be used to search for the desired design, and with appropriate permissions any version of the design can be retrieved to perform an engineering change in a group oriented or individual environment.
- ✓ **Board Fabrication/Assembly** Creation of PCB manufacturing container and check-in of bare board fabrication data and drawings. Check-in of data and drawings for the assembly of boards.
- ✓ **BOM** The product BOM is automatically updated and managed in the PLM system for later transfer to MRP/ERP systems. The variant BOM in PLM contains Reference Designator and, placement data from EDA, and automatically merged mechanical components from the Mechanical CAD design BOM.
- ✓ **Process** **EDA-Layout** uses the PLM release procedures and workflows to manage the status of layout design data. Engineering Change Request workflows and product status reports support time-to-market decisions. Full lifecycle and ECO support.
- ✓ **Variants** Includes support for assembly and programming variants to allow efficient design of families of products. Part alternates and alternate groups are also supported.
- ✓ **Tailorable** The data model, process flows, and release procedure steps can be tailored on-site to match company specific business practices.

Integrate

Benefits

- * Cross-team design coordination. Concurrent engineering can span workgroups and continents!
- * Design release process control. Manufacturing lines and board fabricators receive the right data... the first time!
- * Simplifies compliance with ISO9001, ISO10007, QSA9000, FDA, GMP, and ROHS guidelines!
- * Final Bill-of-Materials extraction to update the BOM in PLM. Fully configurable BOM structure fitting to your companies' processes. Support of BOM redlining and BOM grading.
- * BOM from EDA: Support of assembly variants and programing variants as well as auxiliary mechanical parts like heat sinks.
- * Automatic extraction and versioned check-in of board or panel data set for manufacturing.
- * Extraction and Check-in of variant assembly drawings and of assembly data files into PLM.
- * Check-in of the complete design structure into PLM for engineering changes and design re-use.
- * Works unobtrusively within the familiar EDA tool user interface, so engineers can concentrate on their design activities.
- * Significant gains in data security and capture of data structures.

Supported Systems	Application Versions	Operating System Support ⁽¹⁾			Options Compatibility
		Windows	Solaris	HP-UX	
Altium					
Board Layout	99SE+, PMX	NT 4.0, 2000+, XP			Board Fabrication/Assembly
P-CAD PCB	2006	NT 4.0, 2000+, XP			Board Fabrication/Assembly
Bartels					
Auto Engineer	6.6	NT 4.0, 2000+, XP	2.5.1, 2.6	10.20, 11	Board Fabrication/Assembly
Cadence Design Systems					
Allegro	97A, PE14, SPB 15+	NT 4.0, 2000+, XP	2.5.1, 2.6, 2.7, 2.8, 2.9	10.20, 11	Board Fabrication/Assembly
Orcad PCB	7, 8, 9.2, 10	NT 4.0, 2000+, XP			Board Fabrication/Assembly
Integra					
Integra Station	all	NT 4.0, 2000+, XP			Board Fabrication/Assembly
Mentor Graphics					
Board Station Fablink	EN2005	NT 4.0, 2000+, XP	2.5.1, 2.6, 2.7, 2.8, 2.9	9.05, 10.20, 11	Board Fabrication/Assembly
Expedition Layout	WG 2005	NT 4.0, 2000+, XP			
Pads (Mentor Graphics)					
PCB	5.0+				Board Fabrication/Assembly
Power PCB	5, 6, 2005, 2006	NT 4.0, 2000+, XP			Board Fabrication/Assembly
Zuken Redac					
Board Designer	6, 7, 8	NT 4.0, 2000+, XP	2.7, 2.8, 2.9		Board Fabrication/Assembly
CadStar	4.5, 5	NT 4.0, 2000+, XP			Board Fabrication/Assembly
Visula PCB	4.1, 5	NT 4.0, 2000+, XP	2.7, 2.8	11	Board Fabrication/Assembly
Autoboard Theda	4.1.13, 6.1.2		2.9	11	Board Fabrication/Assembly

- * Check with us for other systems.

Integrate

Options

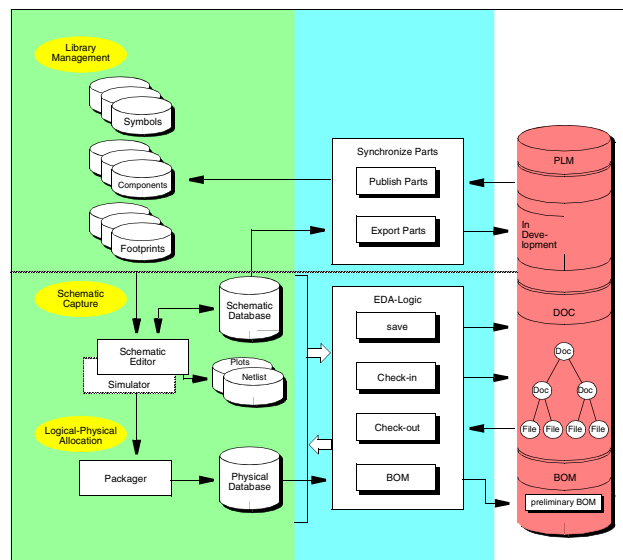
- **Board Fabrication** creates revisioned bare board manufacturing containers. **Board Assembly** combines variants of manufacturing data for the assembly of boards with direct download into assembly machines.
- System design process and data flow automation such as: back-annotation of PLM system **BOM** changes based on Part Number or property changes into the design data, and automatic maintenance in component mapping files.
- **EDA-Logic** and **EDA-Firmware** to automate the entire process and to build consistent, accurate product configurations within the PLM system.

PLM with EDA Logic Capture

EDA-Logic integrates the leading EDA logic capture tools with the PLM system. PLM provides the backbone of product data, configuration, project and workflow management services essential to the successful automation and control of the EDA logic capture data and processes.

The **EDA-Logic** module integrates the task of hierarchical design, file, and library management. Workgroup, enterprise and external communications are supported through the inherently distributed architecture of the PLM system. Features include the automatic extraction of BOMs and attributes (properties) and the implementation of design variants and alternates.

EDA-Logic is based on the JAVA® IUI and works across many platforms. It is integrated with other PLM modules such as the PLM BOM module, Project Management [or PPM], and Product Collaboration.



Functionality

- ✓ **Synchronize Parts** Optionally bidirectional synchronisation of component data with PLM. This includes release control, component grading for instance for ROHS, COST, or release state, and part usage cross references.
- ✓ **Check-in** Check-in of design data with user defined file level resolution along with creation and check of metadata. Data, library and post-processing files are linked to a versioned Document in the PLM system and configured with mechanical and product documentation data for a complete, versioned representation of the product.
- ✓ **Check-out/Get** Search and retrieval of design data, with all dependencies, directly from the PLM system into the EDA working environment. Any of the PLM system attributes can be used to search for the desired design, and with appropriate permissions any revision of the design can be retrieved to perform an engineering change. Support of group-oriented or individual design tasks.
- ✓ **BOM** The product BOM is automatically extracted and managed in the PLM system for later transfer to MRP/ERP systems and to production. The PLM BOM contains Reference Designator data from EDA and automatically merged mechanical components from the Mechanical CAD design BOM. Redlining and BOM grading are supported.
- ✓ **Process** **EDA-Logic** uses the PLM history mechanism, release procedures and lifecycle to manage the status of logic design data. Engineering Change Request workflows and the communication with vendors and manufacturing are easily implemented with full lifecycle and ECO support.
- ✓ **Variants** Includes support for assembly and programming variants to allow efficient design and manufacturing of families of products. Part alternates and alternate groups are also supported.
- ✓ **Tailorable** The data model, process flows, and release procedure steps can be configured on-site to match company specific business practices.

Integrate

Benefits

- * Cross-team design coordination. Concurrent engineering can span workgroups and continents!
- * Design release process control. Purchasing and ODM receive the right data...the first time!
- * Simplifies compliance with ISO9001, ISO10007, QSA9000, FDA, GMP, and ROHS guidelines!
- * Bidirectional synchronisation of metadata.
- * Full synchronisation of EDA electronic item descriptions with classified items in PLM through Synchronize Parts.
- * Advance material disposition with BOMs extracted from packaged schematics.
- * Check-in of the complete design structure for engineering changes and re-use.
- * Automatic extraction of schematic and pcb plot data for visualization throughout the enterprise.
- * Full support of assembly and programming variants in the Bill-of-Materials and plot data.
- * Works unobtrusively within the familiar EDA tool user interface, so engineers can focus on their design activities.
- * Full support of pre-programmed and of in-system programmed parts.
- * Significant automation benefits and synergy effects.

Supported Systems	Application Versions	Operating System Support ⁽¹⁾			Options Compatibility
		Windows	Solaris	HP-UX	
Altium					
Protel Capture	99SE+, PMX, 2002, 2004	95, 98, NT 4.0, 2000+, XP			EDA_Librarian
P_CAD Schematics	2004/5/6	2000+, XP			EDA_Librarian
Bartels					
Auto Engineer	6.6	NT 4.0, 2000+, XP	2.5.1, 2.6	10.20, 11	EDA_Librarian
Cadence Design Systems					
Concept (Scald)	97A	NT 4.0, 2000+, XP (PE 14)	2.5.1, 2.6, 2.7, 2.8	10.20, 11	Star*Select EDA_Librarian
Concept_hdl	SPB13.6 - 15+	NT 4.0, 2000+, XP	2.7, 2.8, 2.9		EDA_Librarian
Composer	Opus 4.4+		2.5.1, 2.6		EDA_Librarian
Mentor Graphics					
Expedition Design Capture	WG 2004/5	NT 4.0, 2000+, XP			EDA_Librarian
DMGR, DA, LMS (opt.)*, BA (opt). Package or To Layout	EN 2002 EN 2004 EN 2005	NT 4.0, 2000+, XP	2.5.1, 2.6, 2.7, 2.8, 2.9	9.05, 10.20, 11	Star*Select EDA_Librarian
DXDesigner/DXDatabase or Pads PCB Designer	2004/5	NT 4.0, 2000+, XP	2.5 - 2.9		EDA_Librarian
OrCAD (Cadence)					
Capture	7, 8, 9.2, 10	98, NT 4.0, 2000+, XP			EDA_Librarian
Pads (Mentor)					
Logic	4, 5				EDA_Librarian
Power Logic	5.0+, 2004/5	98, NT 4.0, 2000+, XP			EDA_Librarian
VeriBest					
Design Capture / Expedition Capture	97A, 98A, 99A-, 2000, WG 2000.5 WG 2002	NT 4.0, 2000+, XP	2.6, 2.8		EDA_Librarian
Zuken Redac					
SCM (XRINF)	5.0.4		2.7+	9.05, 10.20, 11	EDA_Librarian
CR3000/5000 System Designer	5.0.4, 6, 7, 8	NT 4.0, 2000+, XP	2.7+	9.05, 10.20, 11	EDA_Librarian
CadStar	4.5, 5	95, 98, NT 4.0, 2000+, XP			EDA_Librarian

- * Check with us for other systems.

Integrate

Options

- **EDA-Librarian** with the subsets **Publish Parts** and **Export Parts** for bidirectional library management including control of symbols, attributes, part status, part release procedure and processes for an PLM-centered part development workflow.
- **Star*Select** for drag-and-drop of library component symbols from the PLM system directly into the schematic capture tools. Uses the **EDA-Librarian**'s classification system to assist in part selection.
- System design process and data flow automation such as: back-annotation of PLM system BOM changes based on Part Number or property changes into the design data with **bom_back**, and automatic maintenance of component mapping files.
- **EDA-Layout** and **EDA-Firmware** to automate the entire process and to build consistent, accurate product configurations within the PLM system.

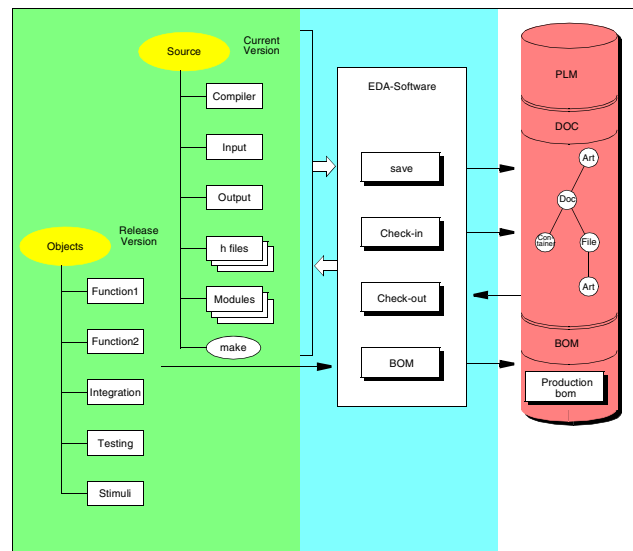
PLM and Software Design

EDA-Software integrates software design systems based on the change management of source and executable code development with the PLM systems. The PLM system provides the backbone for project data, configuration, and workflow management services essential to the successful integration and control of the software design data and processes into a complete project consisting of 3D CAD data, electronic data, software structures, and documentation.

The **EDA-Software** modules support integration of distributed software design environments with hardware design processes. Engineering changes in the project caused by software revisions are fully supported. Workgroup, enterprise and external communications are enhanced through the inherently distributed architecture in the PLM system. Features include the automatic extraction of software source and object module structures and the implementation of bill-of-materials of software items for production.

The **EDA-Software** interface is based on the JAVA® IUI and works across many platforms. It is integrated

with other PLM modules such as the PLM BOM module, Project Management [or PPM], and Product Collaboration.



Functionality

- ✓ **Check-in** Check-in of design environment with user defined file level resolution and indexed version control, along with the check and creation of metadata and make files. Source data and object data files are linked to a versioned Document in the PLM system and optionally configured together with hardware design data for a complete, versioned representation of innovation and product data, such as object code structures.
- ✓ **Check-out** Search and retrieval of the design data structure, with all dependencies, directly from the PLM system into the software design environment for immediate use. PLM system attributes can be used to search for the desired design, and with appropriate permissions, any version of the design can be retrieved to perform an engineering change or re-use of the software module.
- ✓ **Process** **EDA-Software** uses the PLM release procedures and workflows to manage the status of design data. Engineering Change Request workflows and product status reports support time-to-market decisions.
- ✓ **Tailorable** The data model, process flows, and release procedure steps can be configured on-site to match company specific business practices.
- ✓ **BOM** Creation and update of a bill-of-materials structure with the objects of the software system, including accessories like media and label.

Integrate

Benefits

- * Support of product data management of software design, electronic design, mechanical design, and documentation.
- * Cross-team design synchronisation. Concurrent engineering can span design applications in all your subsidiaries.
- * Design release process control. customers, manufacturing, and vendors receive the right data the first time!
- * Simplifies compliance with ISO9001, ISO10007, QSA9000, FDA and GMP guidelines.
- * Software configuration management and release procedures are fully supported.
- * Compliant with software development systems of leading suppliers.
- * Continue to use the software design system as previously - unaffected by the integration.

Supported Systems

EDA-Software is compliant with software design systems such as ClearCase, PVCS, SCCS, RCS, and various other case tools. As an alternative solution, the integration supports directly configuration and version control of native software design environments. **EDA-Software** is available with the operating systems Solaris 2.5.1, 2.6-2.9, HP-UX 10.20, HP-UX 11, Windows NT 4.0, Windows 2000, and Windows XP.

Options

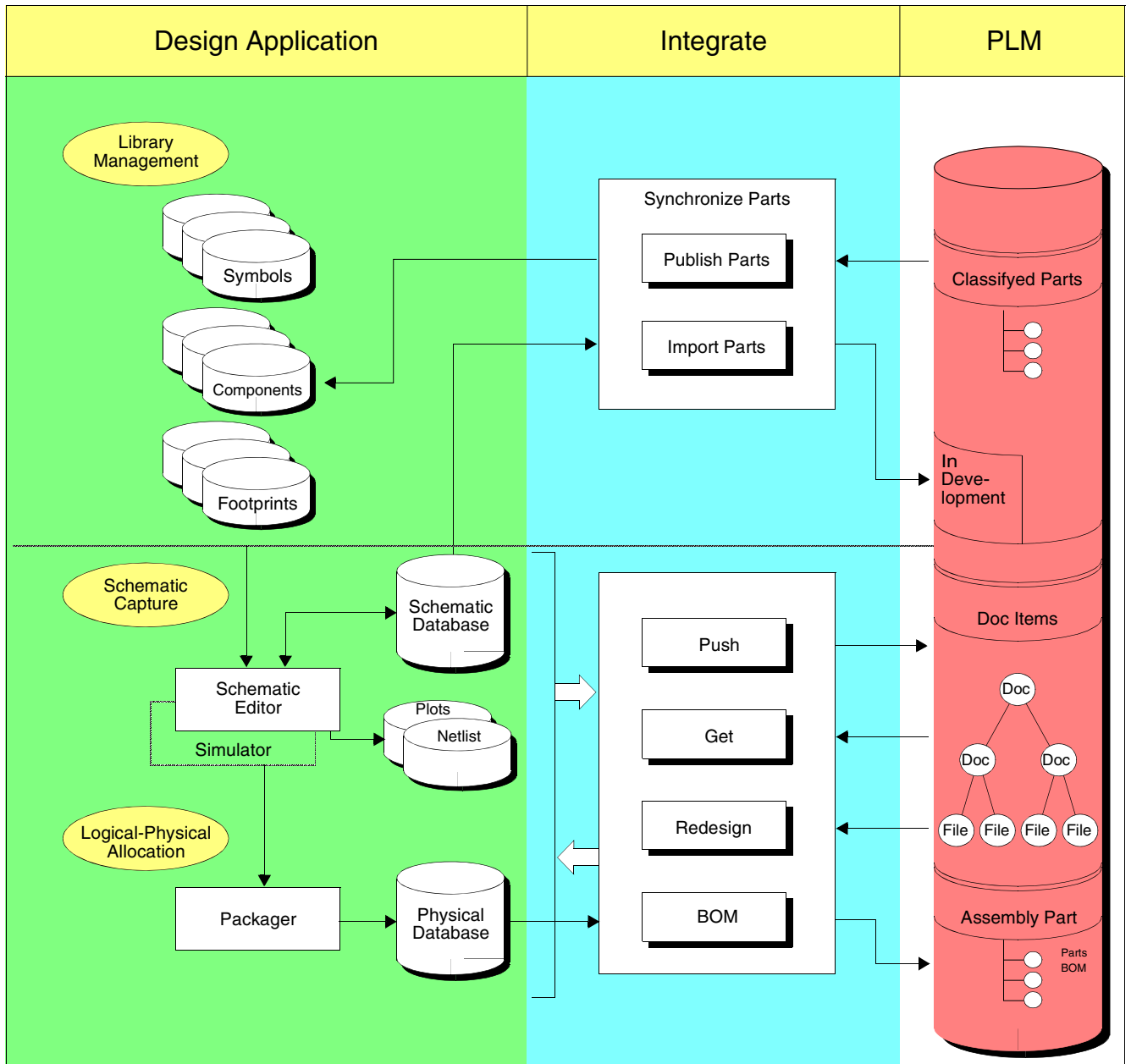
EDA-Logic and **EDA-Layout** to automate the combined hardware–software design process and to build consistent, accurate product configurations within the PLM system.

Integrate

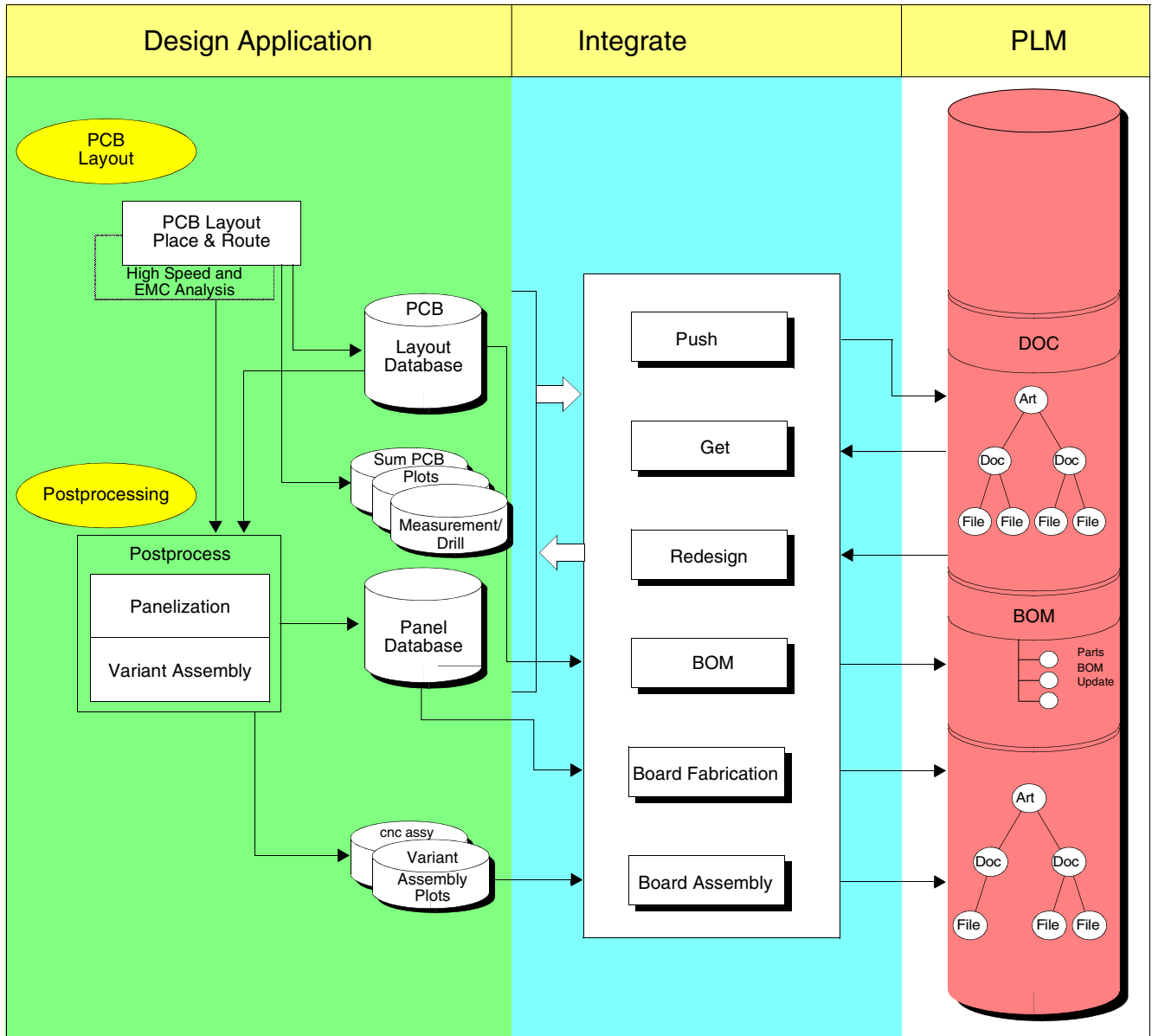
The Integration of Design Systems with PLM

Presentation V1.9

EDA-Librarian and EDA-Logic



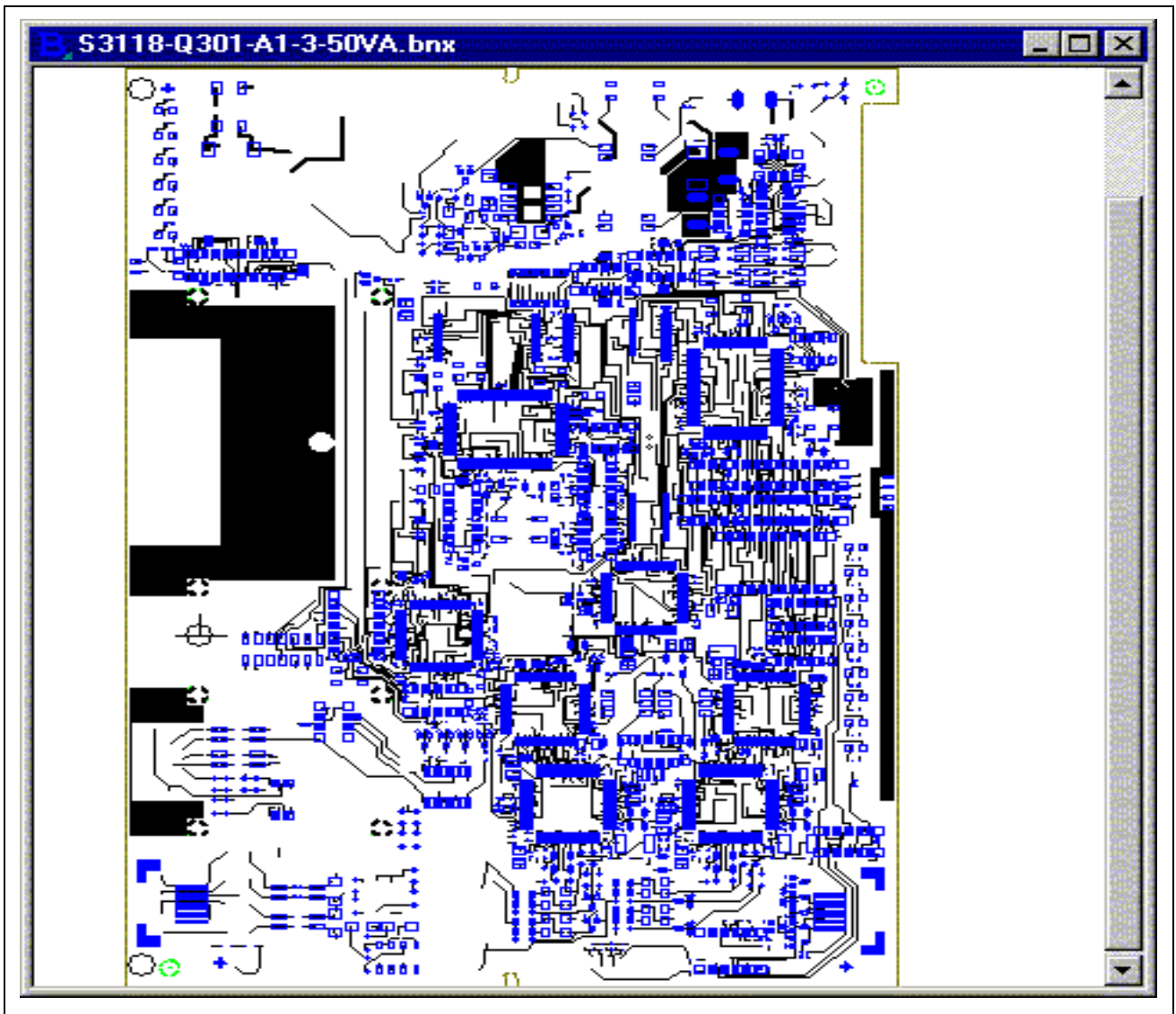
EDA-Layout



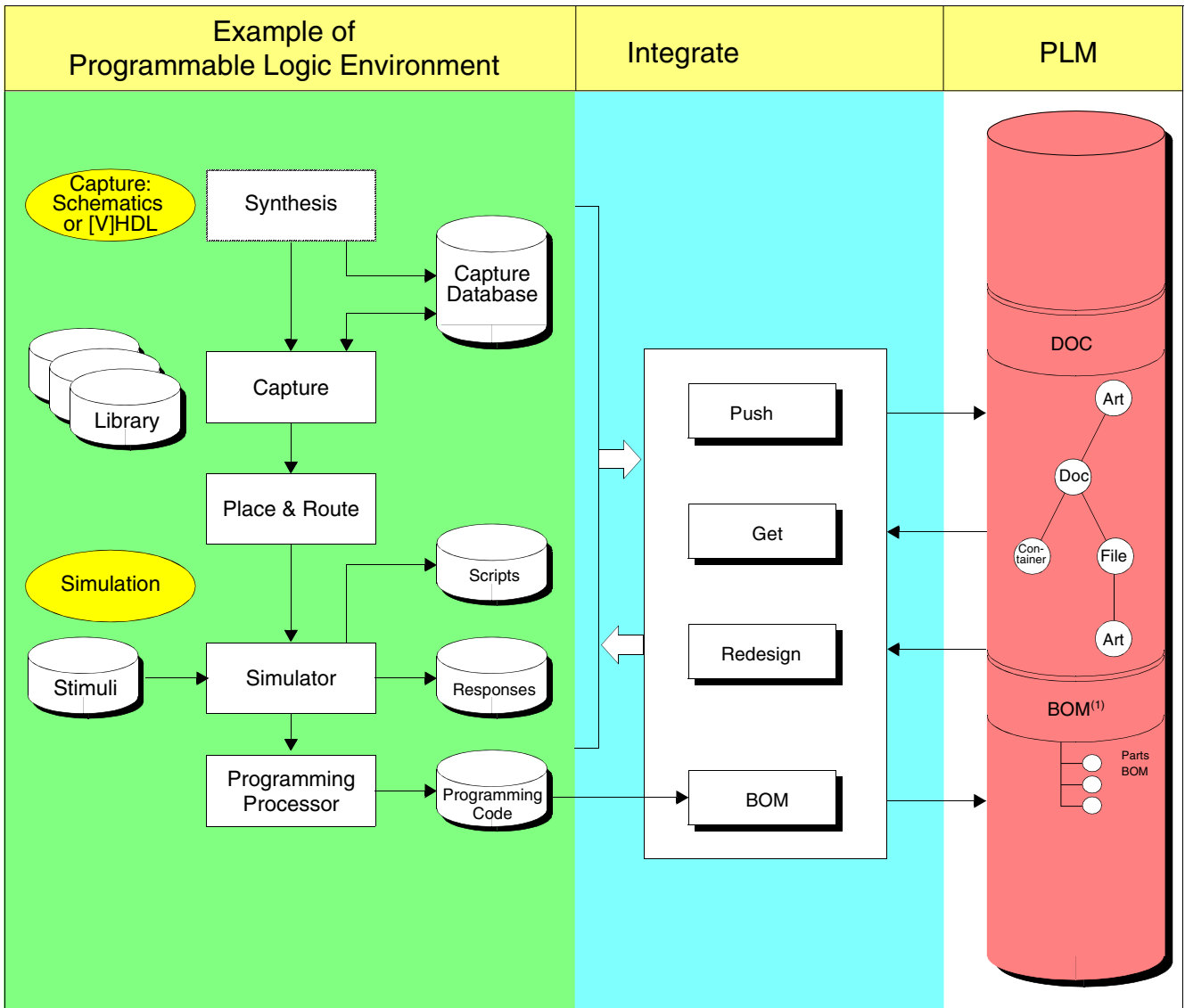
Plus: Push/Redesign Mech Mechanical Data for exchange with 3D board assembly data.

Example of Data handled by the Integration

Printed Circuit Board Layout



EDA-Firmware



(1) With label, media, bar code, etc.



Shown: FPGA Design environment.



Also available with the [F_EP]ROM programming environment, and with CPLD environments.

Example of Data handled by the Integration



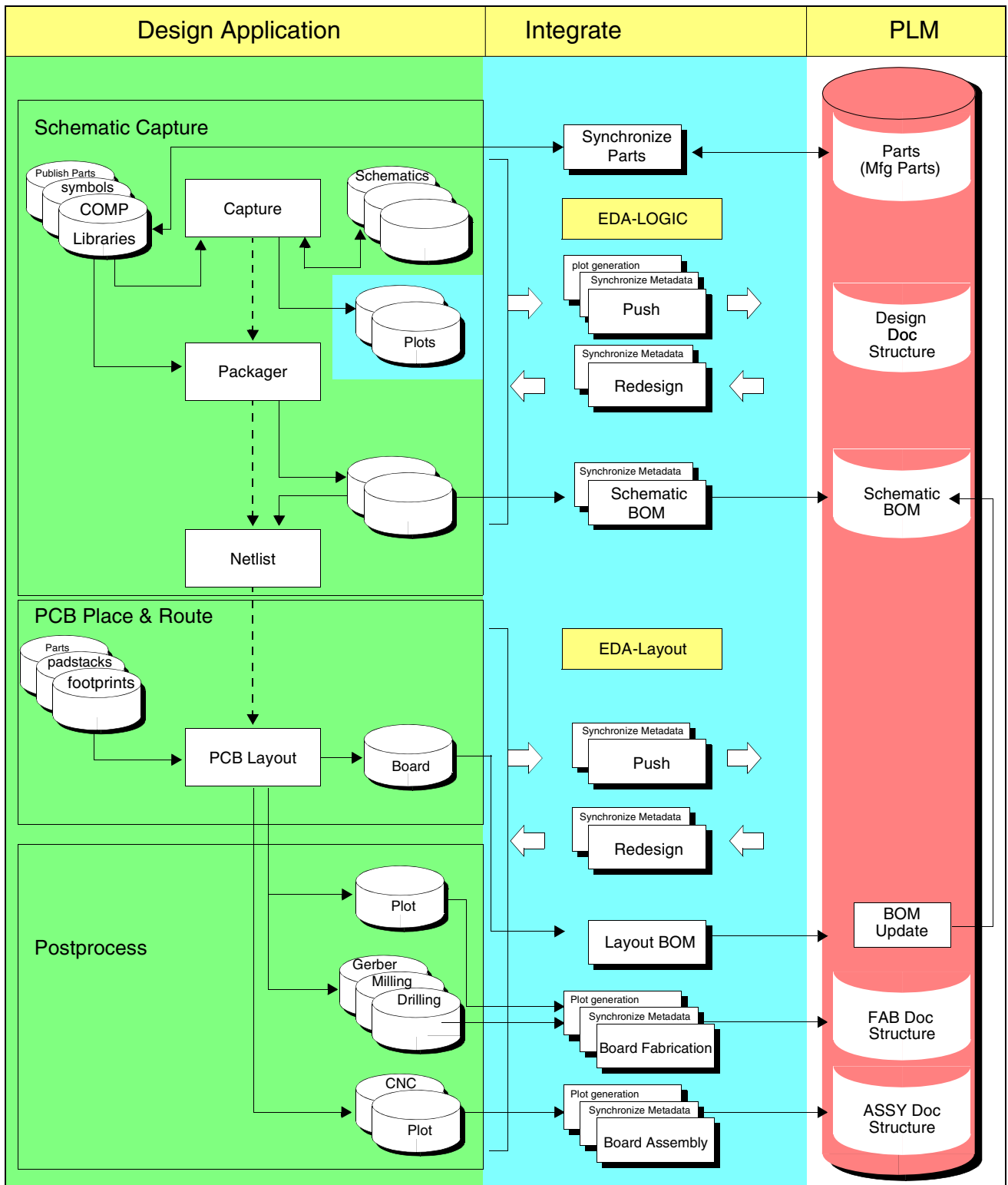
Pinning File

```
#####
# Pin Map Table for Design Netlist: top
#####
# Design Port name      LMC pin identifier  Direction  Package pin
# -----
#
# Input ports:
DAT2                IO6                IN          28
CARRYIN             IO12               IN          37
CLR                 IO13               IN          38
A0_IN               IO15               IN          40
B1IN                IO17               IN          42
DAT1                IO18               IN          43
B0_IN               IO23               IN          48
A1IN                IO27               IN          59
ENA                 IO41               IN          8
CLKIN               IO47               IN          14
XRESET              RST                IN          20
#
# Output ports:
OMQ<0>              IO0                OUT         22
OMQ<1>              IO1                OUT         23
OMQ<2>              IO2                OUT         24
OMQ<7>              IO3                OUT         25
OMQ<4>              IO4                OUT         26
OMQ<5>              IO5                OUT         27
OMQ<6>              IO10               OUT         32
Q3                  IO16               OUT         41
Q6                  IO19               OUT         44
FF20OUT             IO20               OUT         45
Q4                  IO21               OUT         46
Q5                  IO22               OUT         47
FF1OUT             IO24               OUT         56
OUT2                IO25               OUT         57
CLKOUT              IO26               OUT         58
OUT1                IO30               OUT         62
Q7                  IO31               OUT         63
OUT3                IO32               OUT         64
Q1                  IO34               OUT         66
Q0                  IO37               OUT         4
FF1AOUT             IO38               OUT         5
Q2                  IO39               OUT         6
OMQ<3>              IO43               OUT         10
#
# Bidirectional ports:
FF20AOUT            IO33               IO          65
FF1A0OUT            IO35               IO          67
#
# Unused symbol pins:
INPUT4              INPUT4             NC          2
INPUT5              INPUT5             NC          15
.
.
.
```



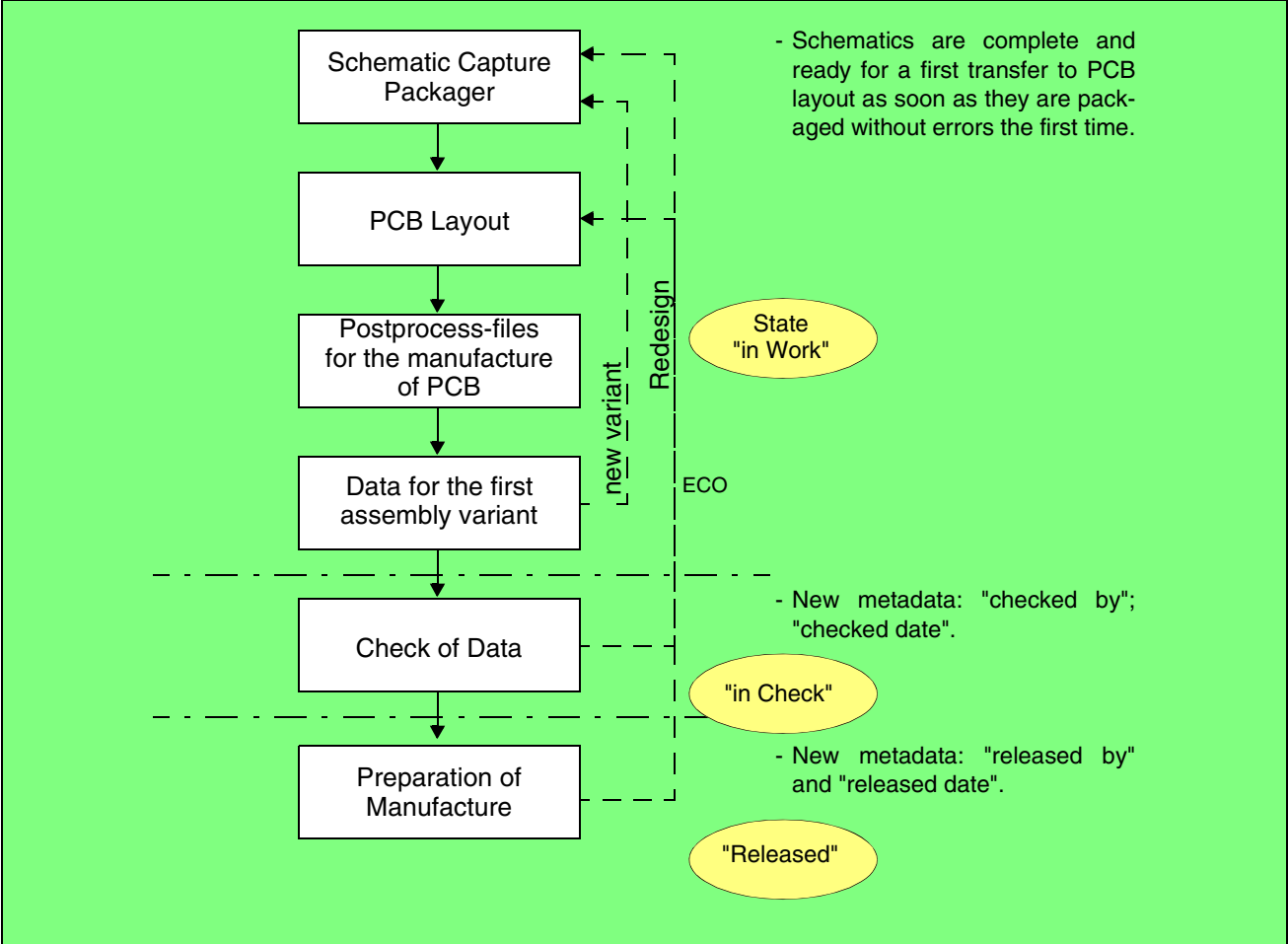
Automatic Generation of a Symbol.

The integrated Design Process



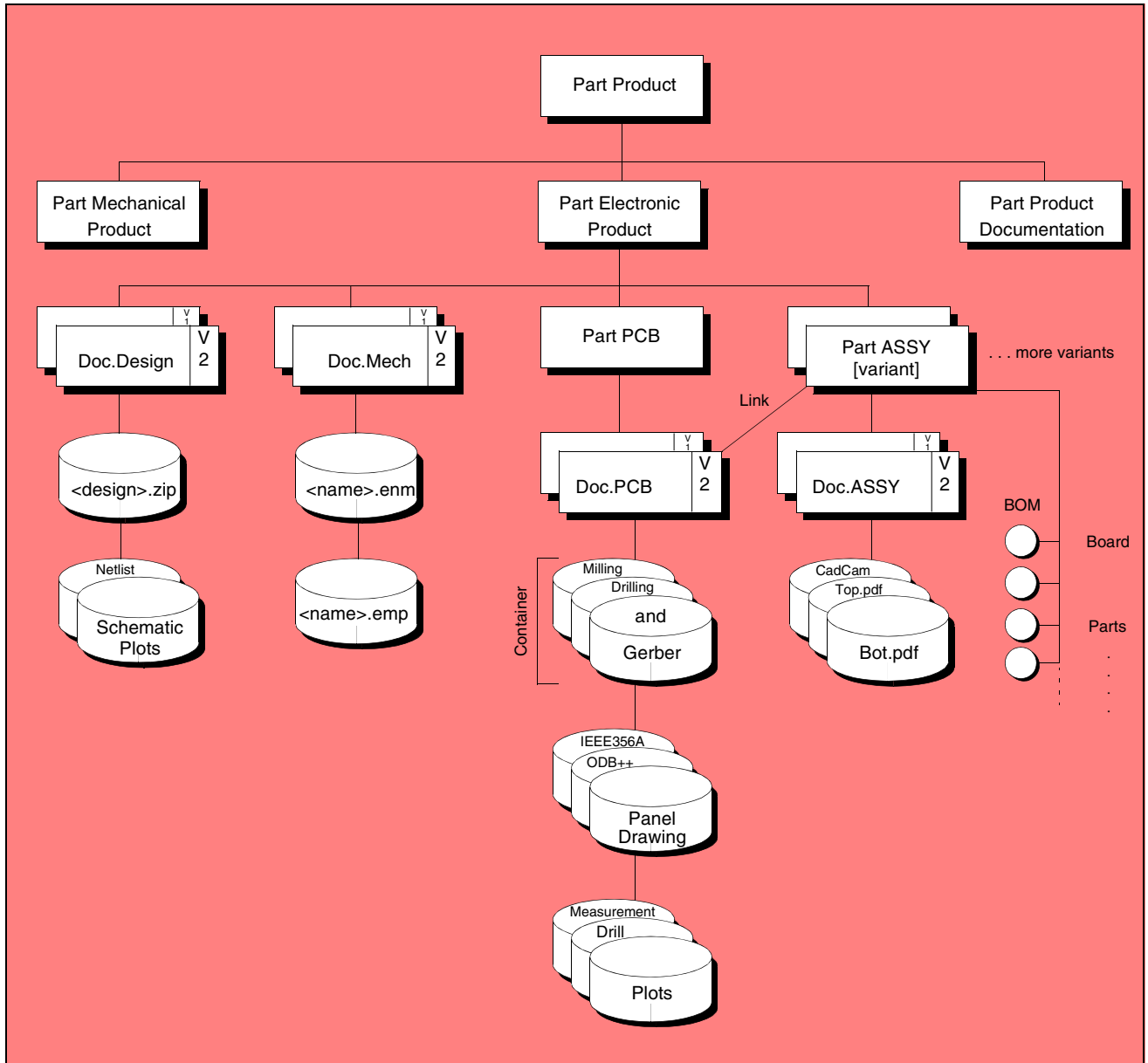
Automated extraction and synchronisation of data in the design application.

The Design Workflow



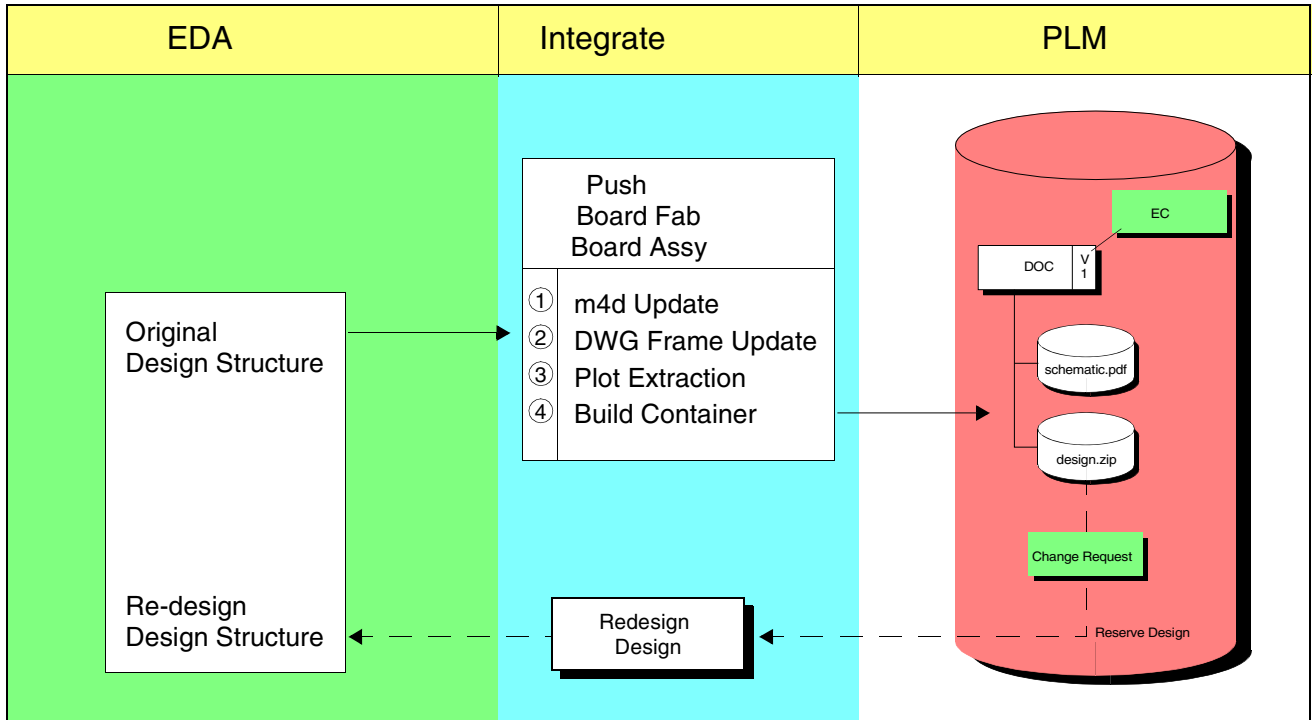
Data Model in PLM

Example of the data model of an electronic product.



EC Cycle

Engineering Change and Innovation Data



❑ **The EC Process controls revisioning and workflow in PLM.**

❑ **Redesign reserves the design to prevent simultaneous modifications by other engineers. Redesign refreshes the revision and the EC history in design data. In contrast Get allows fetching of any design.**

❑ **Functional Blocks and Designs provide a function design library in PLM.**

Synchronize Metadata



Use case 1: The data model pre-exists in PLM. Synchronize Metadata supports placement of metadata from PLM in the design structure. This process typically occurs just once, before the first execution of the corresponding Integrate module.



Use case 2: The data model is created by the Integrate. In this case Synchronize Metadata builds the complete data model in PLM.



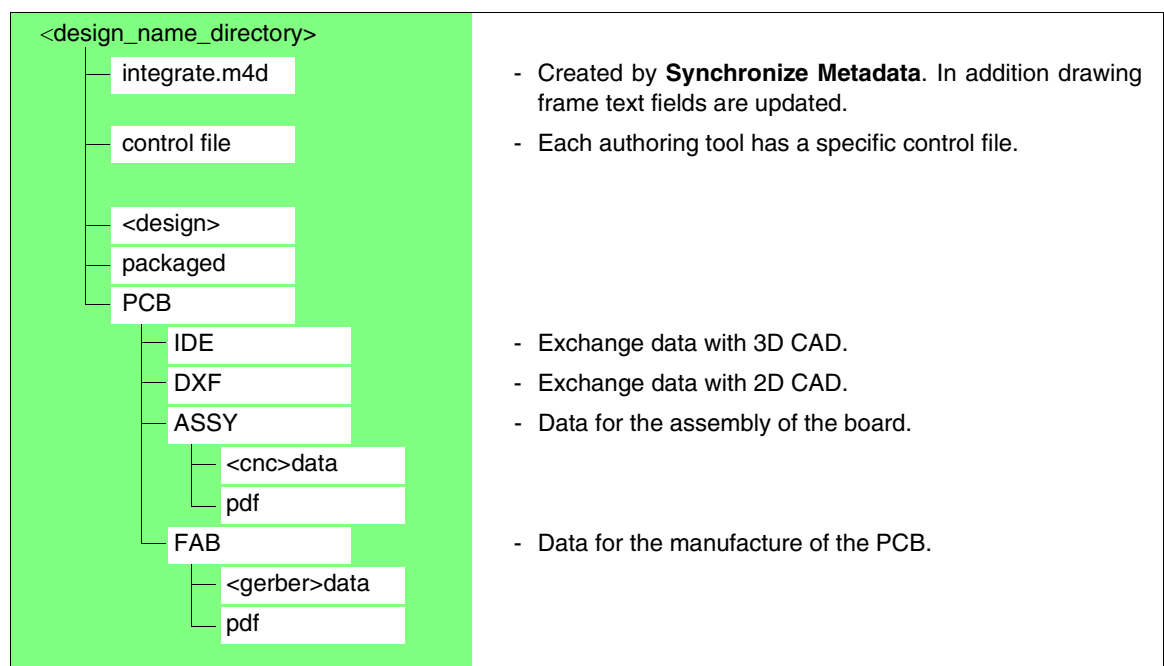
Refresh: Update of metadata in the design with each module execution.



Optionally create design structure in the file system.



Example of a Design Structure



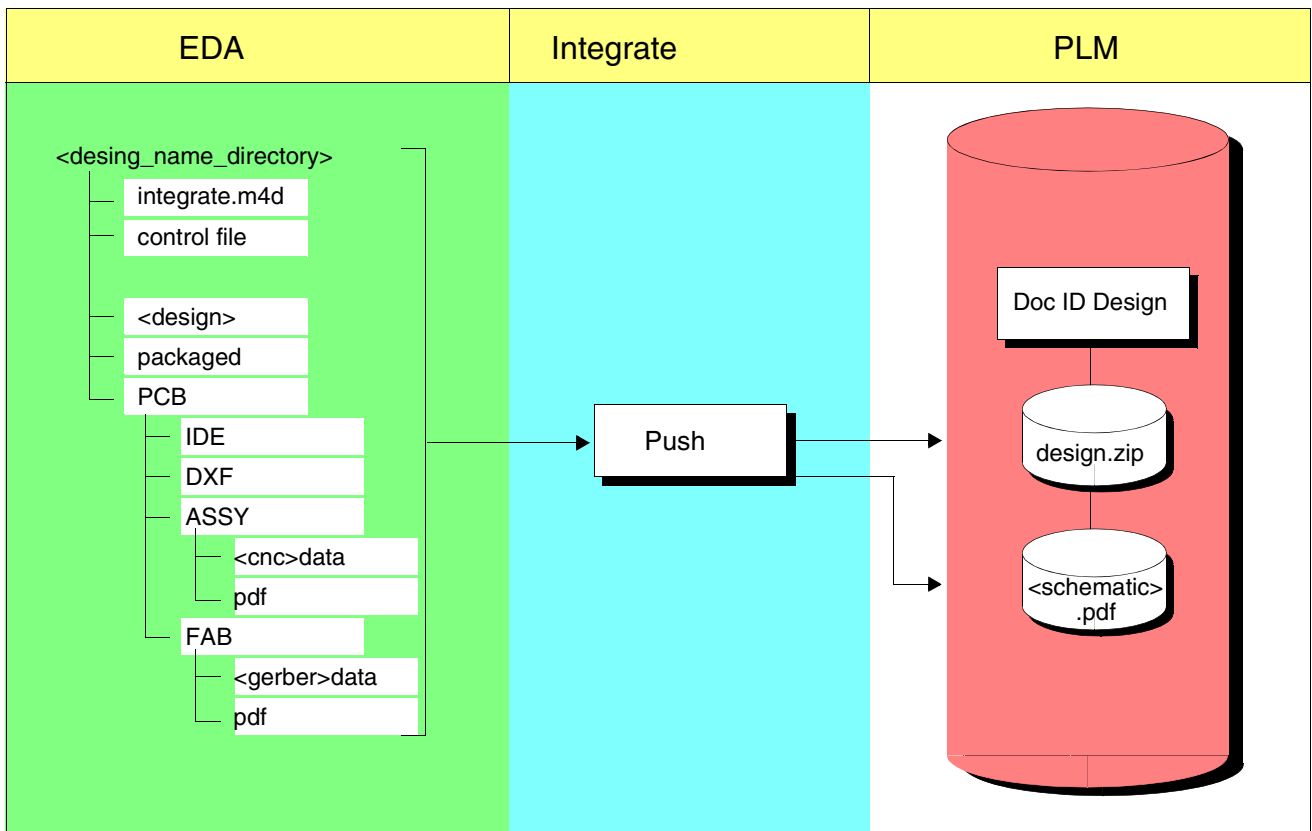
Synchronize Metadata



The Front-API of Push updates drawing frame properties with metadata such as drawing number and version. The Update occurs on all schematic pages and on PCB drawings of the design.

Push

- ❑ **Push maintains document data of Schematic Capture and PCB Layout in PLM.**
- ❑ **Push creates plot data from schematics and saves design data in PLM.**
- ❑ **Example of a Design Structure and Push**



- ❑ **Push may create an ECO in PLM.**
- ❑ **Various configurable options like Engineering Release, archiving of design with design library, increase version.**

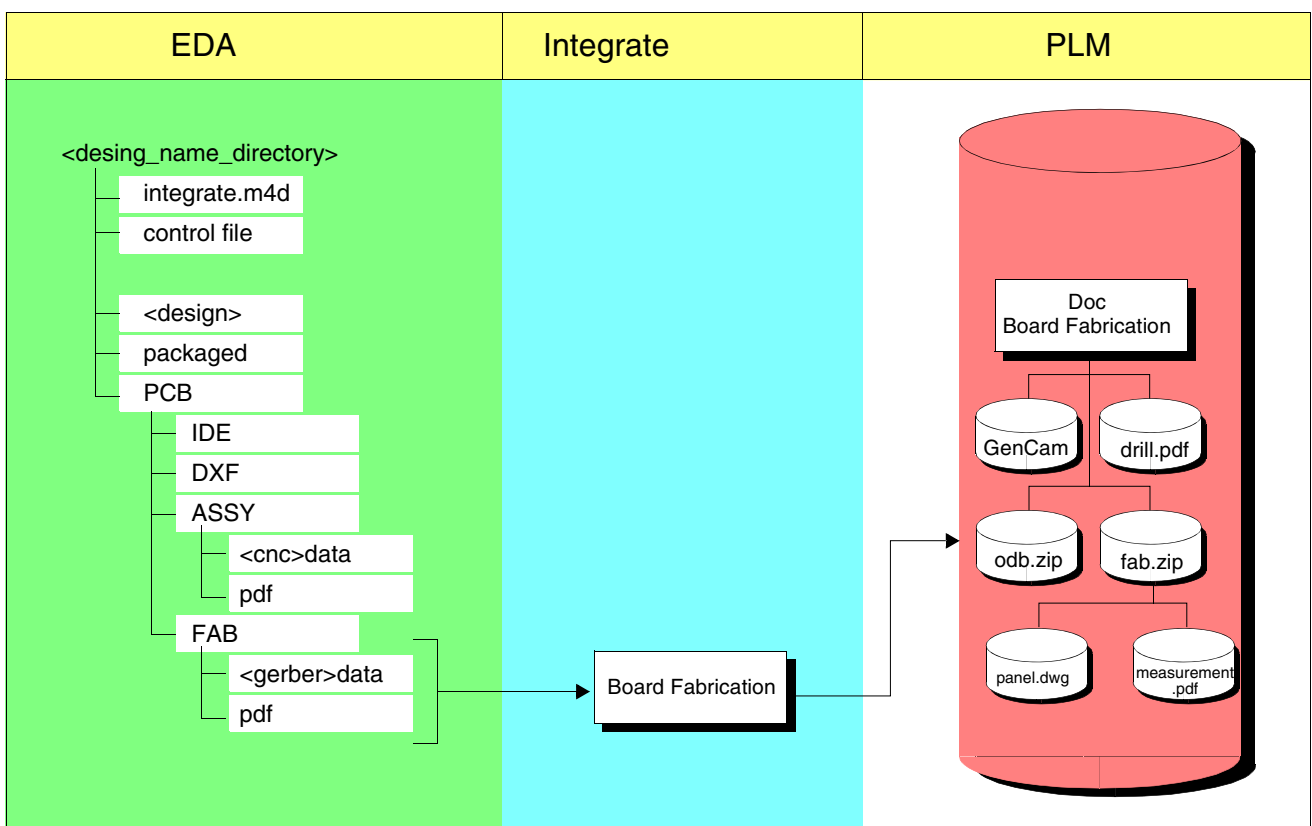
Redesign / Get

- ❑ **Redesign resolves design containers into the EDA environment which were stored in PLM with Push.**
- ❑ **Redesign reserves the innovation document with the data of the authoring EDA system in PLM for this user and increases the revision putting the design document into the "in work" state in PLM.**
- ❑ **Get checks out without reservation and sets metadata to the initial state.**
- ❑ **Refresh of Metadata: revision, EC, change history.**

Board Fabrication

❑ The Integration module Board Fabrication is used to check manufacturing data of the bare board into PLM. Data include the FAB container with Gerber data and related data, and plot files.

❑ Design Structure and Board Fabrication



❑ Layer control by view files in the extraction Process.

❑ Optionally layer stackup extracted.

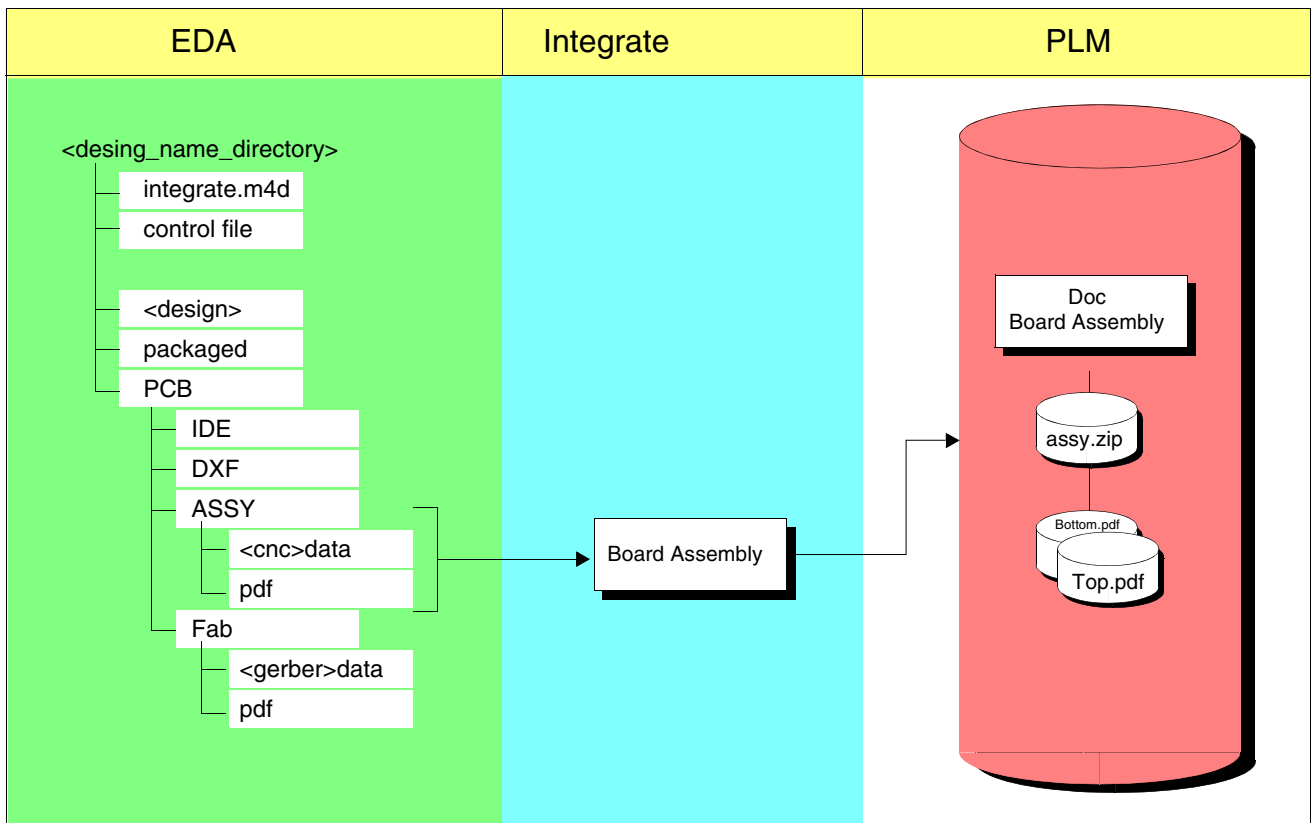
❑ Optional ODB++ output.

❑ Optional GenCam output.

Board Assembly

❑ The module is used to check data for the assembly of the board into *assy.zip* in PLM. It creates and picks up *pdf* files out of the *ASSY* subdirectory and checks these in as separate files which can be viewed in the PLM client.

❑ Example of a Design Structure and Board Assembly



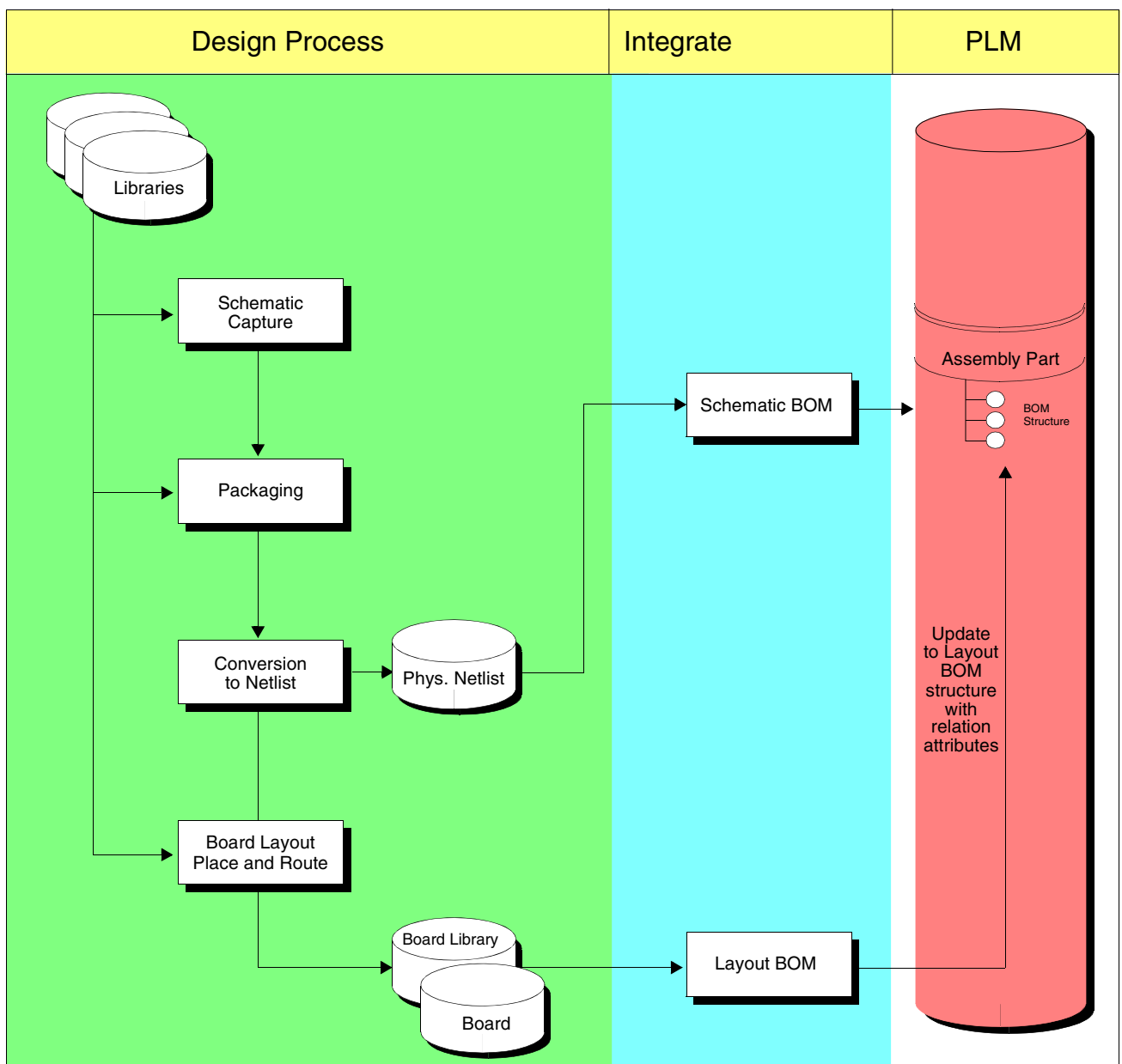
❑ Extraction of optimized CNC files for Assembly control.

❑ Optional extraction of variant schematic plots.

BOM

❑ The BOM function creates a Bill-of-Materials structure with parts in PLM.

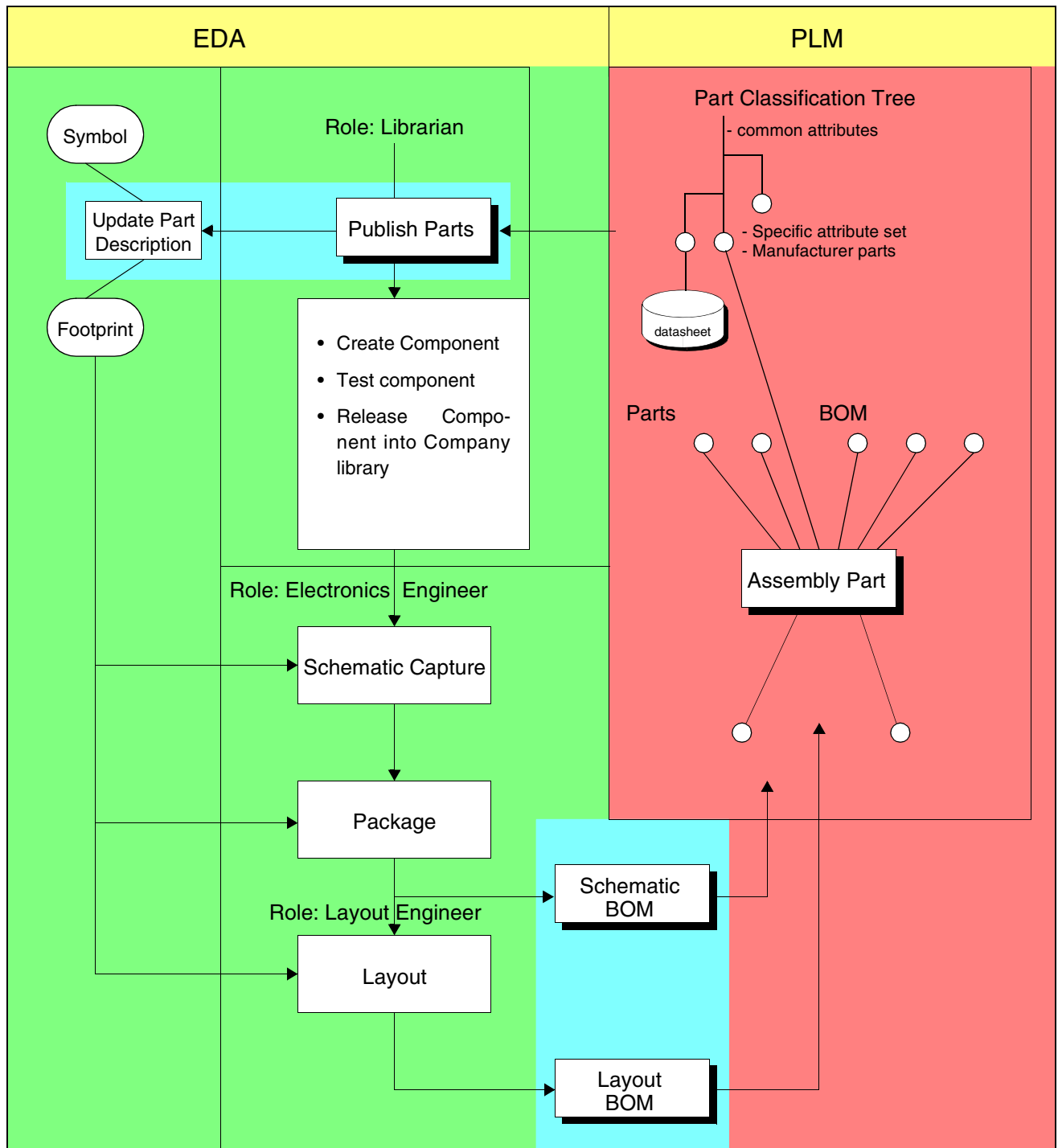
❑ Example of a Design Process with BOM



Example of a Configuration

- ❑ **Upon the first execution, BOM creates values for the find number. In subsequent updates, BOM retains these numbers.**
- ❑ **Schematic BOM just places `POS_NO`, `PART_NO`, `REFDES` and `QUANTITY` in the BOM tables. Layout BOM optionally adds the component location information.**
- ❑ **BOM supports accessory parts, variant BOMs, and substructures for pre-programmed devices.**
- ❑ **Variant BOMs are based on assembly and on firmware variants.**
- ❑ **Configurable to support substructures for the mounting technologies Manual, THT, and SMD.**

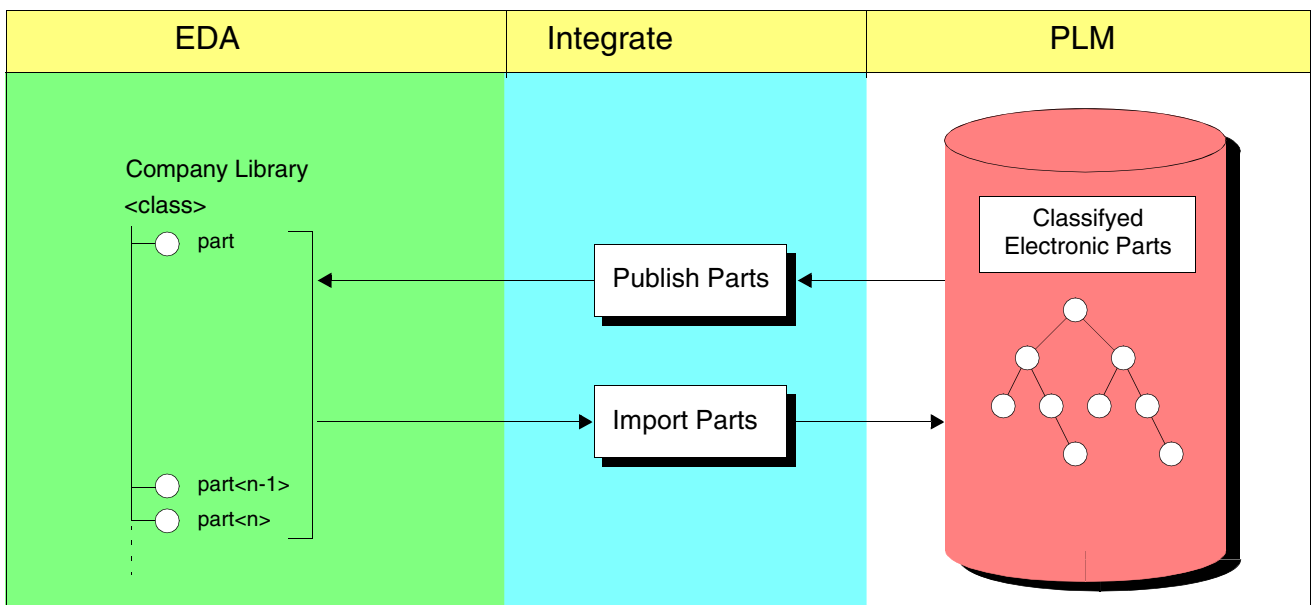
Synchronisation of Part and BOM DATA



Synchronize Parts



Update of [classified] Parts with Publish Parts.



Update Layout Libraries



Display list of affected designs.



Update and display data sheets.



Import Parts to create pending parts from EDA in PLM.



Special handling of attributes like release state.



Support of URL-based viewing of data sheets.

Synchronize Parts



Synchronize Parts Main Window

Library Path:

Available Classes

- Miscellaneous-Battery
- IC
- Diode
- Transistor
- ASIC
- Resistor-const**
- Resistor-Potentiometer
- Resistor-Trimmer
- Resistor-NTC
- Resistor-PTC
- Capacitor-Tantalum
- Capacitor-Ceramic
- Inductivity
- Filter
- Acoustic-Receiver
- Acoustic-Microphone
- Mechanical-Switch
- Mechanical-Readcontact
- Mechanical-Jumper
- Mechanical-Connector
- Fuse
- Relay
- Quartz
- Transducer
- Inductor
- Coil-Passive
- Coil-Active

Selected Classes

- Resistor-const

>

>>

<<

<

Window to select classes for comparison.

Update error

Result light:
red: error
yellow: busy
green: complete, no error

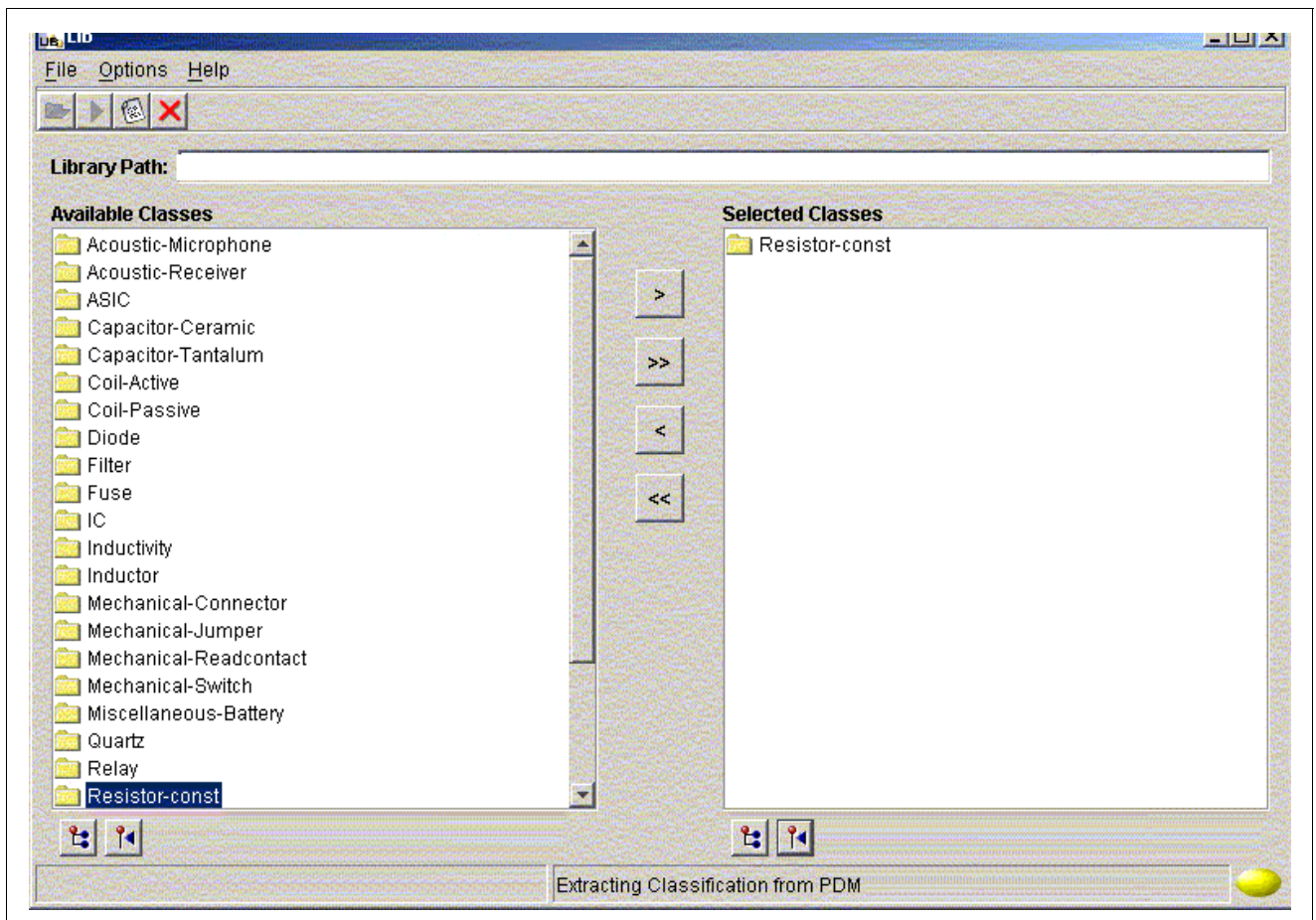
No hierarchy expansion

Expand hierarchy in the display

Available Classes

Synchronize Parts

- **One Class selected for Comparison: Resistor-const**

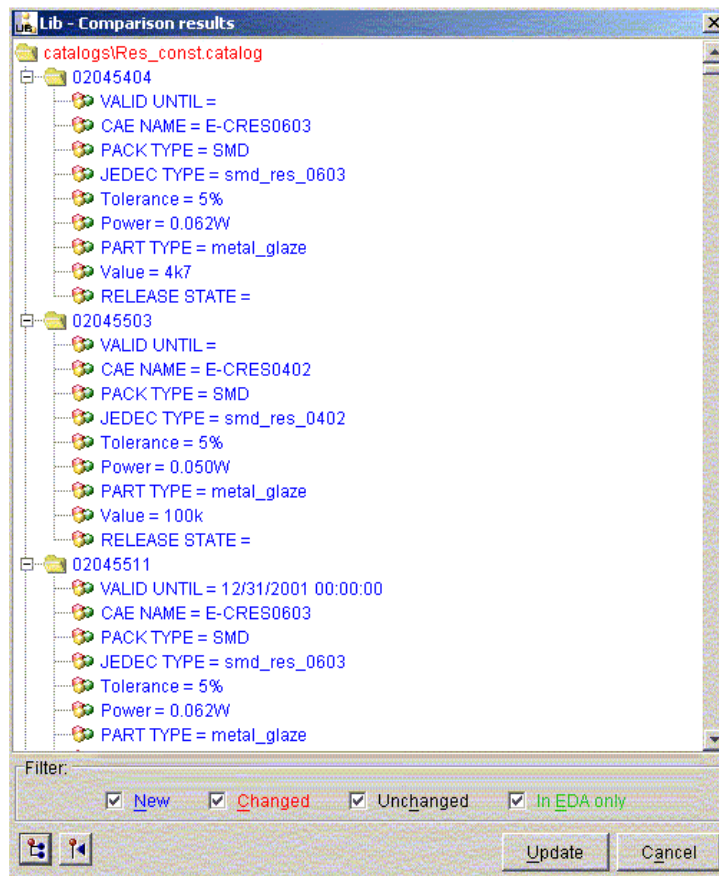


- **Execute the comparison from the  button.**

Synchronize Parts



Comparison Result Window



Synchronize Parts



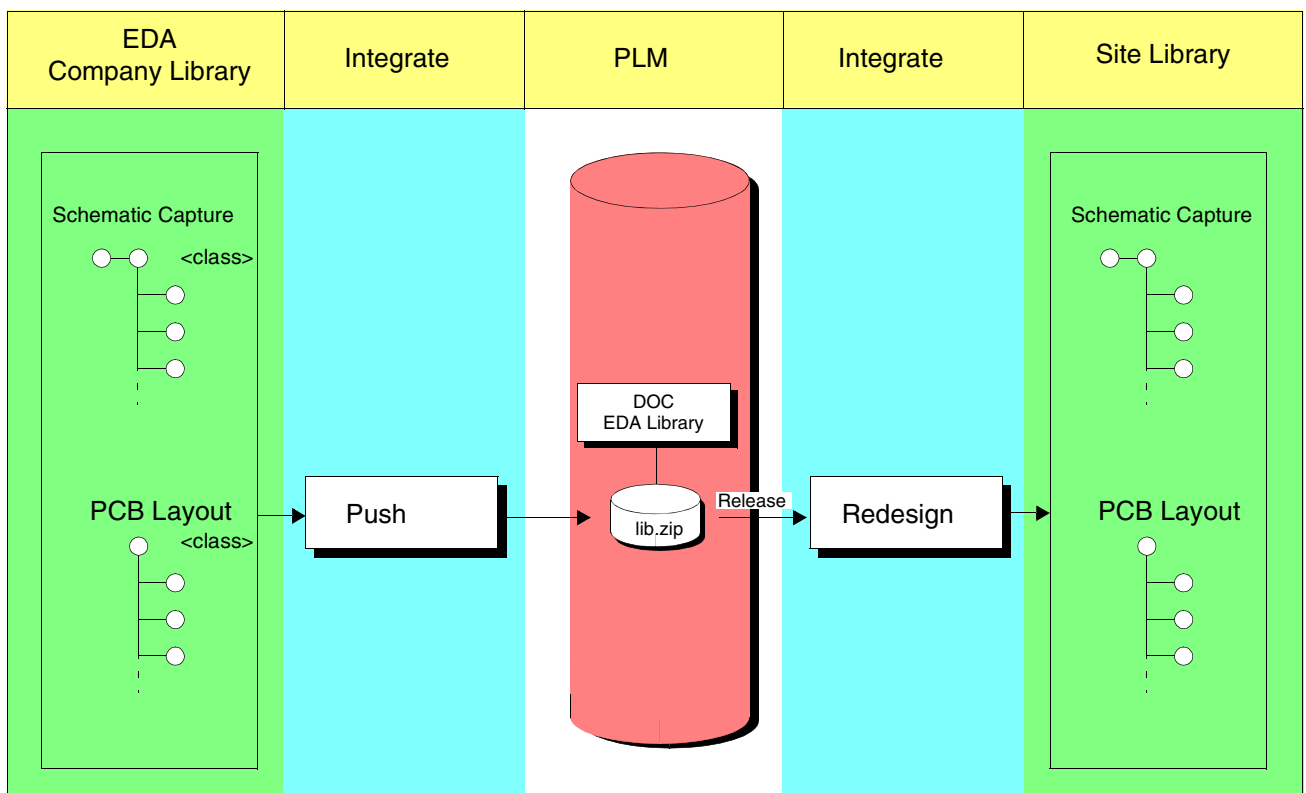
Sample of Classes and Attributes in PLM

Class Name	Attributes
Battery	Release_State Value Type Damping Jedec_Type Assy_Tech. CAE_Name Valid_until
IC	Release_State Value Type Jedec_Type Assy_Tech. CAE_Name Valid_until
Diode	Release_State Value Type Jedec_Type Assy_Tech. CAE_Name Valid_until
Transistor	Release_State Value Type Jedec_Type Assy_Tech. CAE_Name Valid_until
ASIC	Release_State Value Type Jedec_Type Assy_Tech. CAE_Name Valid_until
Resistors	Release_State Value Type Power Tolerance Jedec_Type Assy_Tech. CAE_Name Valid_until
.	
.	
.	

Distribution of Libraries

❑ Push Lib and Redesign Lib are being used to distribute EDA libraries into sites.

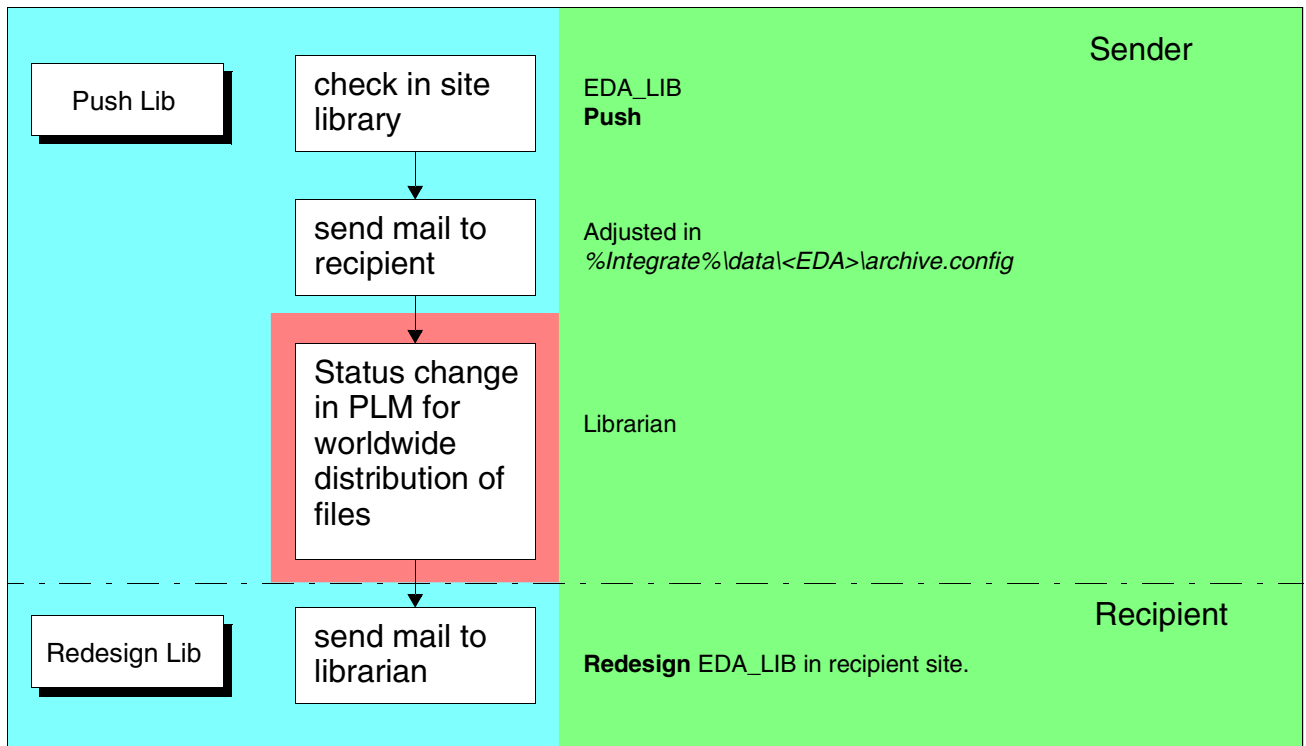
❑ The Data Flow of the Distribution



Operation of the Library Distribution

- ❑ The site library is to be distributed to other sites with Push. It is there downloaded with Redesign.

- ❑ **Library Distribution**



- ❑ **Mail Text and Recipient**
The recipient of the mail and the text is set in *%Integrate%\data\<EDA>larchive.config*.

Good to know: The Process of Introducing the Integration



Configuration Paper

- **Customer design and workflow data**
- **Example BOM**
- **Dump, if available**
- **Build test and configuration environment**
- **Workshop to determine details of the configuration paper**
- **Release the configuration paper**



Configuration of Integrate



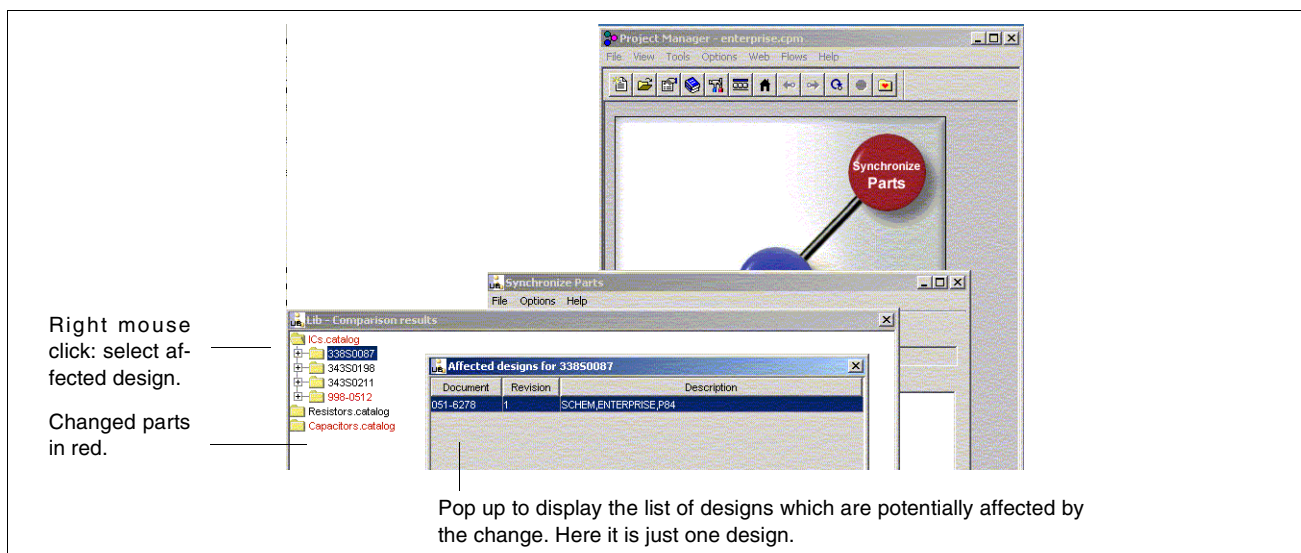
**Installation at the customer site with user's guide
Introduction of the system administrator.**

Interesting Additions

- Approved-Quality level check routines assure checked in data which can be used company wide.**
- bom_back**
Backannotation of edited Bill-of-Material changes from PLM into the EDA design. Changes are offered for import by the design engineer and may be changes of attributes or part numbers.
- Inspect**
The viewing and analysis tool for all downstream process steps like test engineering, production repair, and for [Web based] design collaboration.
- Context**
A graphical tool to compare and modify Bill-of-Materials and document structures: Old version in PLM - new version from EDA - before Push.
- meta4plot**
Update of text in plots from the CCB and released states in PLM.
- Design Grading**
Grade design changes for cost, ROHS, Reliability, ...
- Supplier Package**
Compare product structures as shipped by external suppliers.
Support collaboration based on concurrent visual implementation and structure checks.
- Manufacturing Interfaces**
Download packages into manufacturing machines.

Design Grading - Add a new Dimension to Design Analysis

- ❏ **Synchronize Parts displays part differences between PLM and the EDA library before update. To gauge the result of an update just display the list of affected designs.**

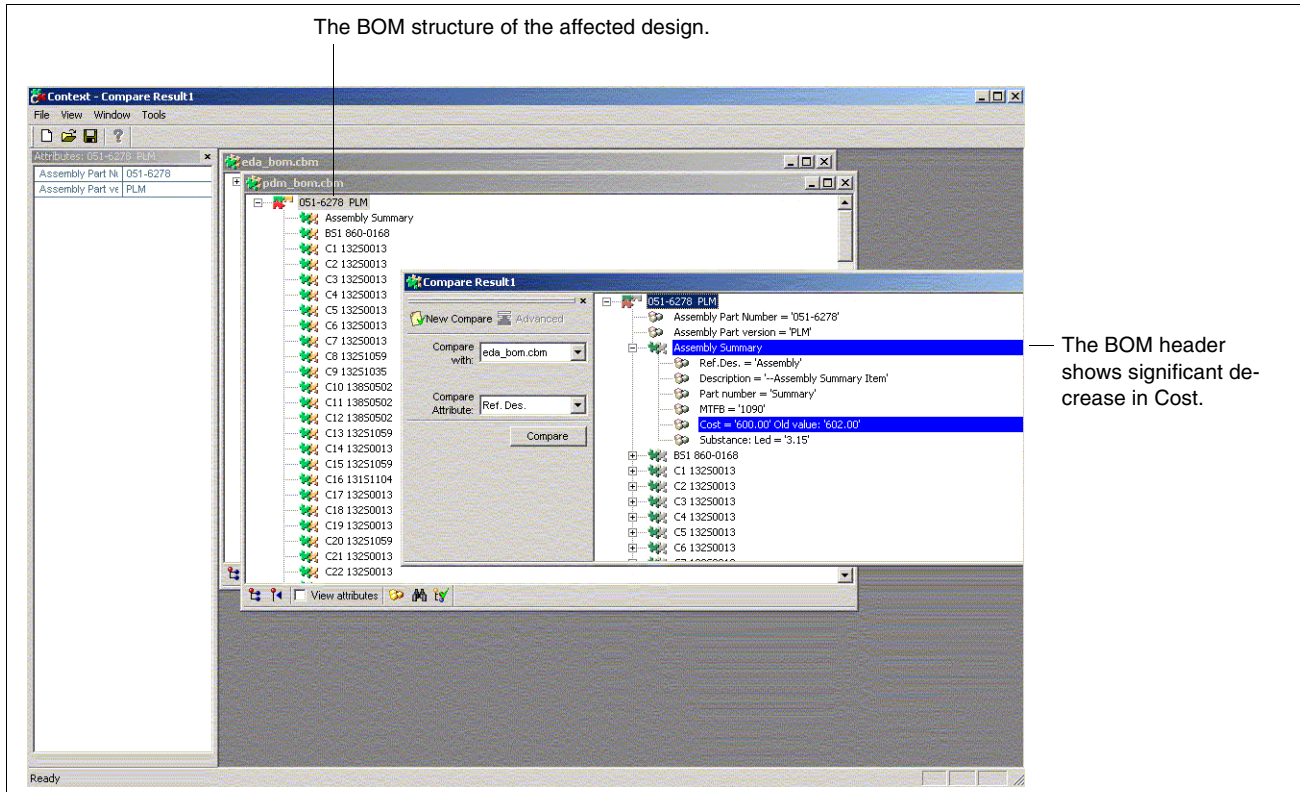


List affected Designs from Changed Parts

- ❏ **Operation of the Details button in the affected designs list causes a comparison window to pop up.**

Design Grading - Add a new Dimension to Design Analysis

The BOM structure of the affected design.



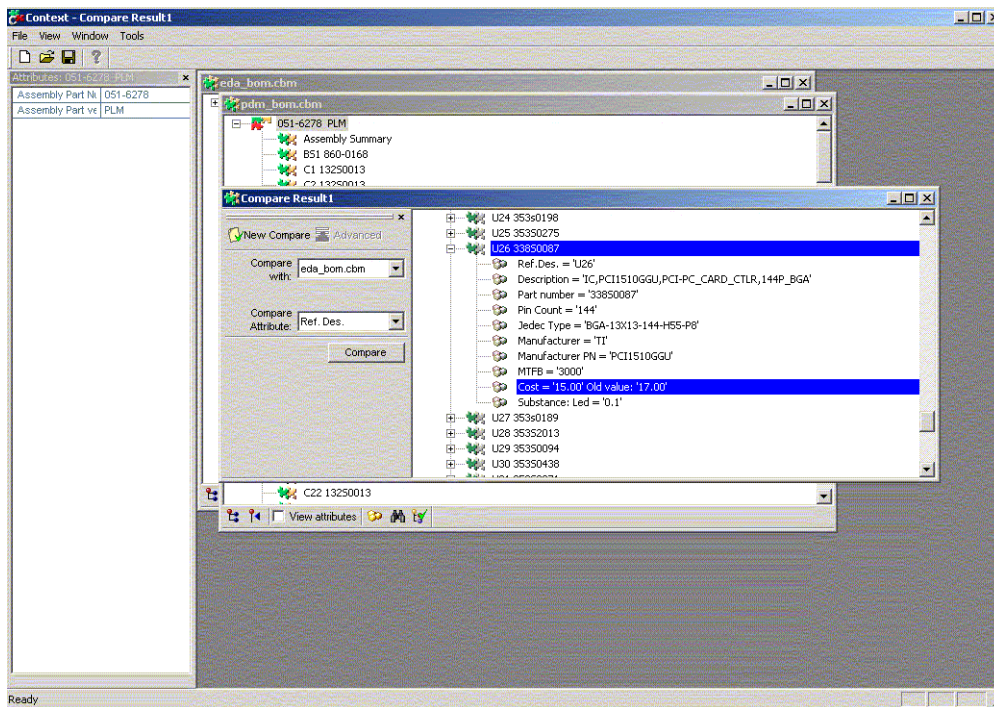
The BOM header shows significant decrease in Cost.

Compare the old and the new Design Contents



The BOM header shows a significant decrease in cost if the part is updated from PLM and used in the EDA library.

Design Grading - Add a new Dimension to Design Analysis



The Part causing the Cost Decrease



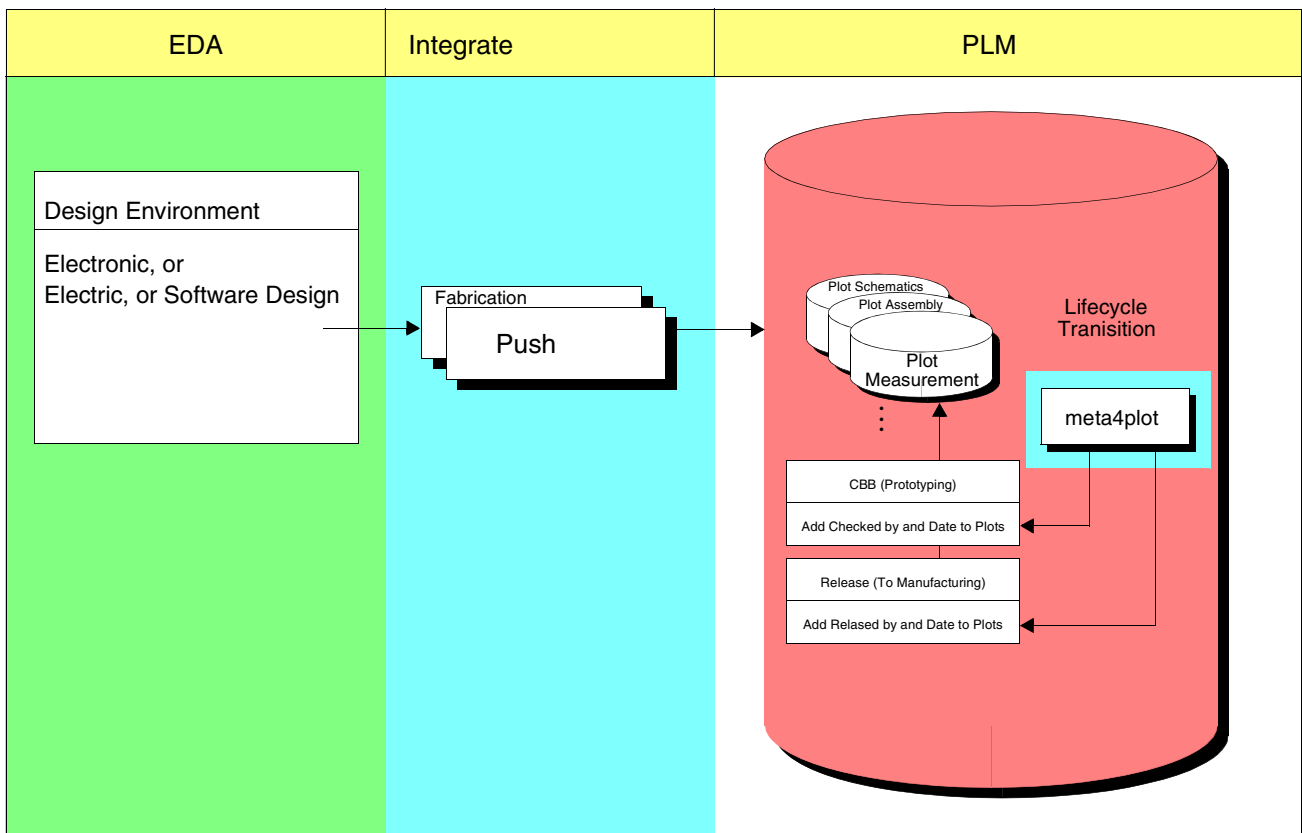
The part is highlighted. It potentially causes a significant decrease of the cost of the design.

Design Grading - Add a new Dimension to Design Analysis

Benefits of Design Grading

- **Grade the Impact of Part updates in Designs for:**
 - **Cost**
 - **MTBF**
 - **ROHS**
 - **End of life components**
 - **EMI**
- ... or another attributes or combinations of attributes.**

Meta4plot - Annotate Metadata into Plot Files with State Change in PLM



Meta4plot - Annotate Metadata into Plot Files with State Change in PLM

Application

- **Push updates drawing border text fields with metadata from PLM, extracts plot files, and checks them in.
The text fields show the author, and date.**
- **An EC in PLM prohibits further checking in of design data.
But it triggers meta4plot to update the plots with name and date of the checking person.**
- **The next transition in the workflow repeats the process with name and date of the releasing person.**

Meta4plot - Annotate Metadata into Plot Files with State Change in PLM

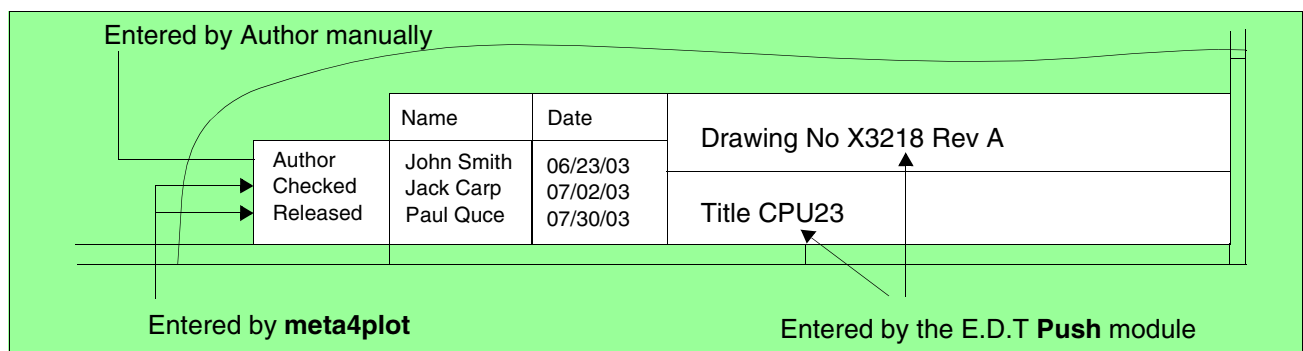
Benefits

- **Construction data like plots display the workflow state.**
- **The design can be modified and reused independent of the original revision.**
- **Configuration options of meta4plot:**
 - **One plot file for all schematics or individual pages.**
 - **Selectable format: pdf or TIFF G4.**
 - **The plot may be in a zip file.**

Meta4plot - Annotate Metadata into Plot Files with State Change in PLM

Operation

- ❑ **meta4plot is started automatically from the PLM server.**



Example of annotated Metadata in the Drawing Frame

- ❑ **Name, initials or the electronic signature is annotated into the drawing frames automatically.**

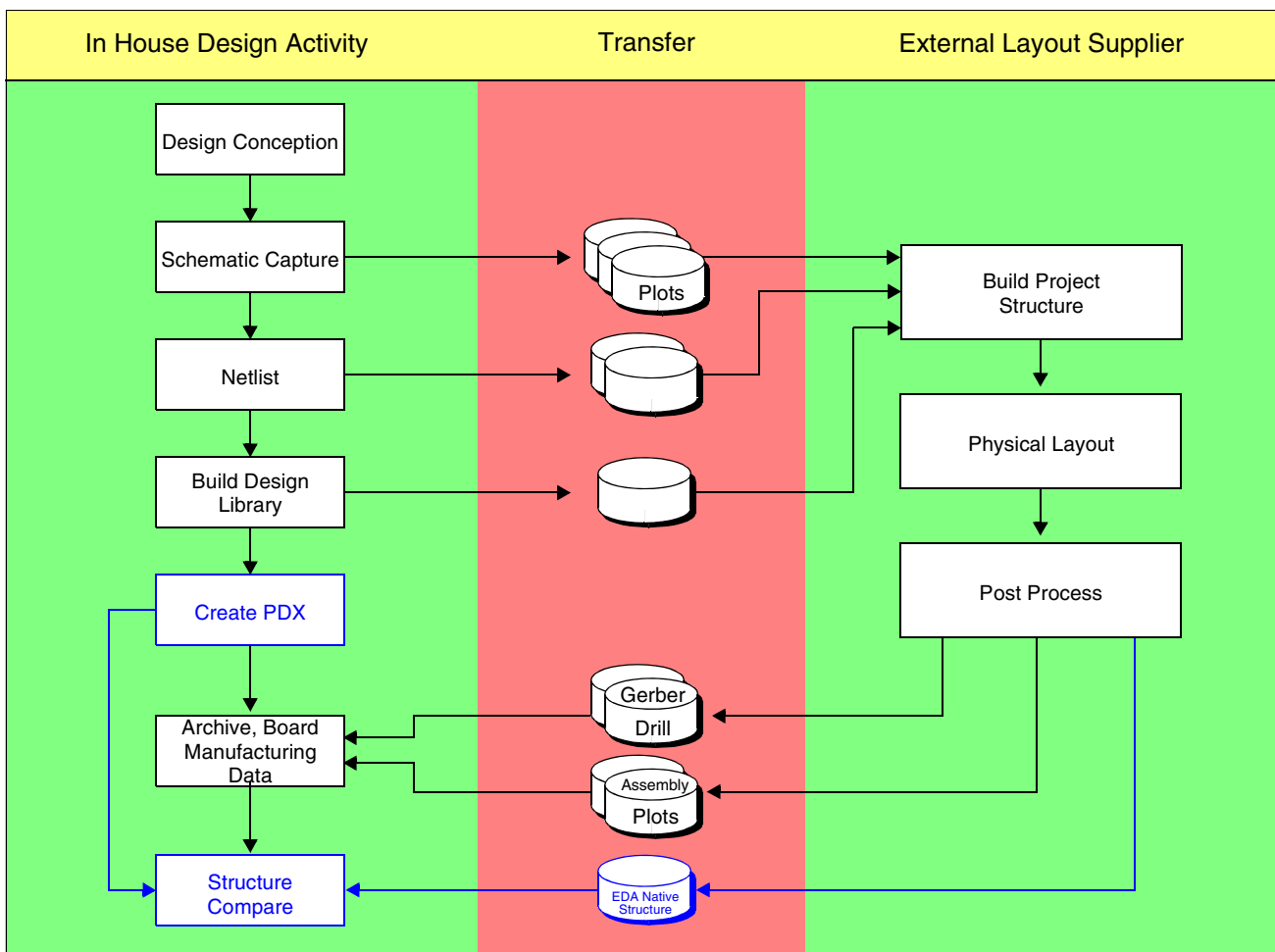
Summary

- ❑ **The meta4plot package is triggered in the PLM server by an EC causing a state change. It annotates configurable metadata into drawing border symbols.**

Design Synchronisation with external Suppliers



Scenario: The schematics are developed in house, the physical layout is developed by an external supplier.



“Extended Workbench” - External Supplier

Design Synchronisation with external Suppliers

- ❑ In the process, external suppliers may have used
 - changed reference designators,
 - different part numbers, especially with added components.

- ❑ The design engineer wants to compare the product structure between the master schematics and the physical layout. PDX is a neutral standard description for product structures.

- ❑ PDX comparison is performed with the Java-based Context4 on any platform.

Design Synchronisation with external Suppliers

RefDes	Part NR	Description	X	Y
R1	10058	RESISTOR, 1.27KW, ±1%, SMD 0603	10,0	11,0
R2	10058	RESISTOR, 1.27KW, ±1%, SMD 0603	10,0	12,0
U3	12048	EMBEDDED LINUX PROCESSOR, PB	11,0	13,0
R4	10059	RESISTOR, 39W, SMD 0603, MARKE	11,0	14,0
	10060	RESISTOR, 8.2W, SMD 0603, MARKE	11,0	14,0
R5	40070	RESISTOR, 0.2W, SMD 0603, MARKE	-11,0	-16,0
U1	12045	10/100BASE-TX/FX TRANSCEIVER, TC	14,0	19,0
U1.1	12096	16K GATES QUICKRAM FPGA, TQFP-1		
U1.2	12098	4-PIN µP VOLTAGE MONITOR WITH M		

Original
 Added
 Changed
 Removed

PDX-based Comparison of two Product Structures

Modified

Part Nr	Description	Qty	POs Nr	Ref Des
10058	RESISTOR, 1.27KW, ±1%, SMD 0603	2,0		R1, R2, R3 ...
10059	RESISTOR, 39W, SMD 0603, MARKE	0		R4 ...
10060	RESISTOR, 8.2W, SMD 0603, MARKE			R4 ...
40070	RESISTOR, 0.2W, SMD 0603, MARKE			R5 ...
12045	10/100BAS			
12096	16K GATES			
12098	4-PIN µP V			

Ref Des Viewer

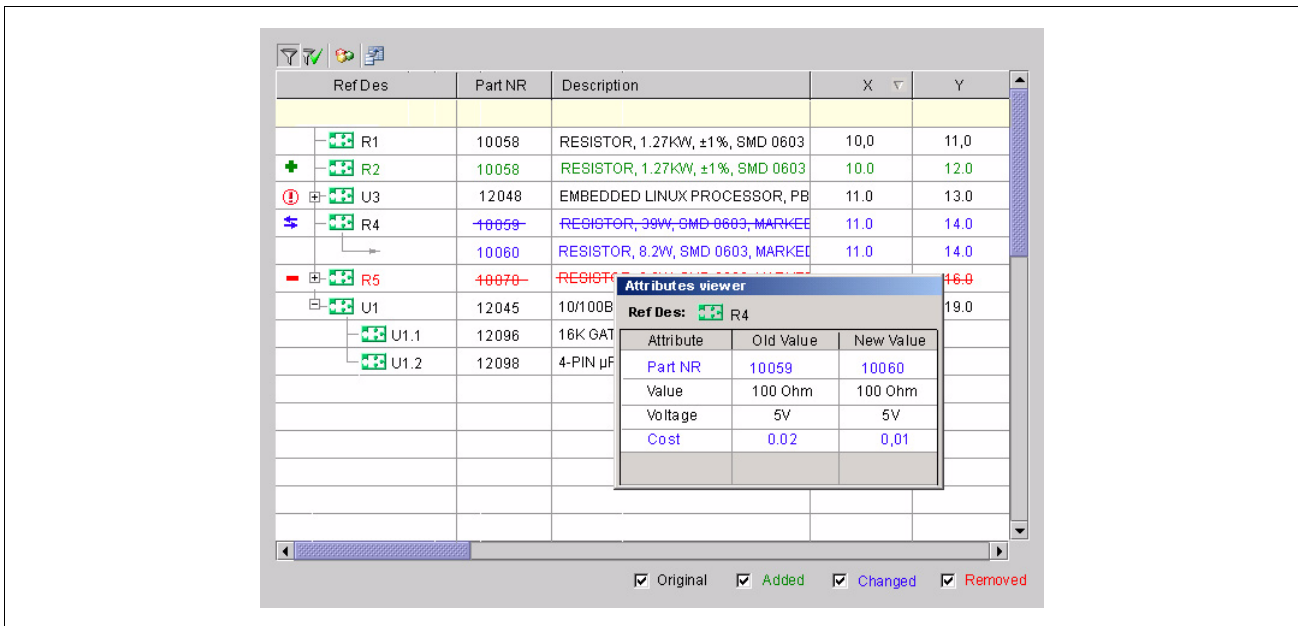
Part Nr: 10058

Ref Des	Action
R1	
R2	Added (modified)
R3	Deleted (modified)

Original
 Added
 Removed

Differences in the changed Product Structure

Design Synchronisation with external Suppliers



View Attributes of the changed Parts



PDX Comparison is based on PDX extractors from schematics and from physical layout tools. These are available for all EDA systems.



The design may be viewed and redlined bi-laterally from any part in the structure display.